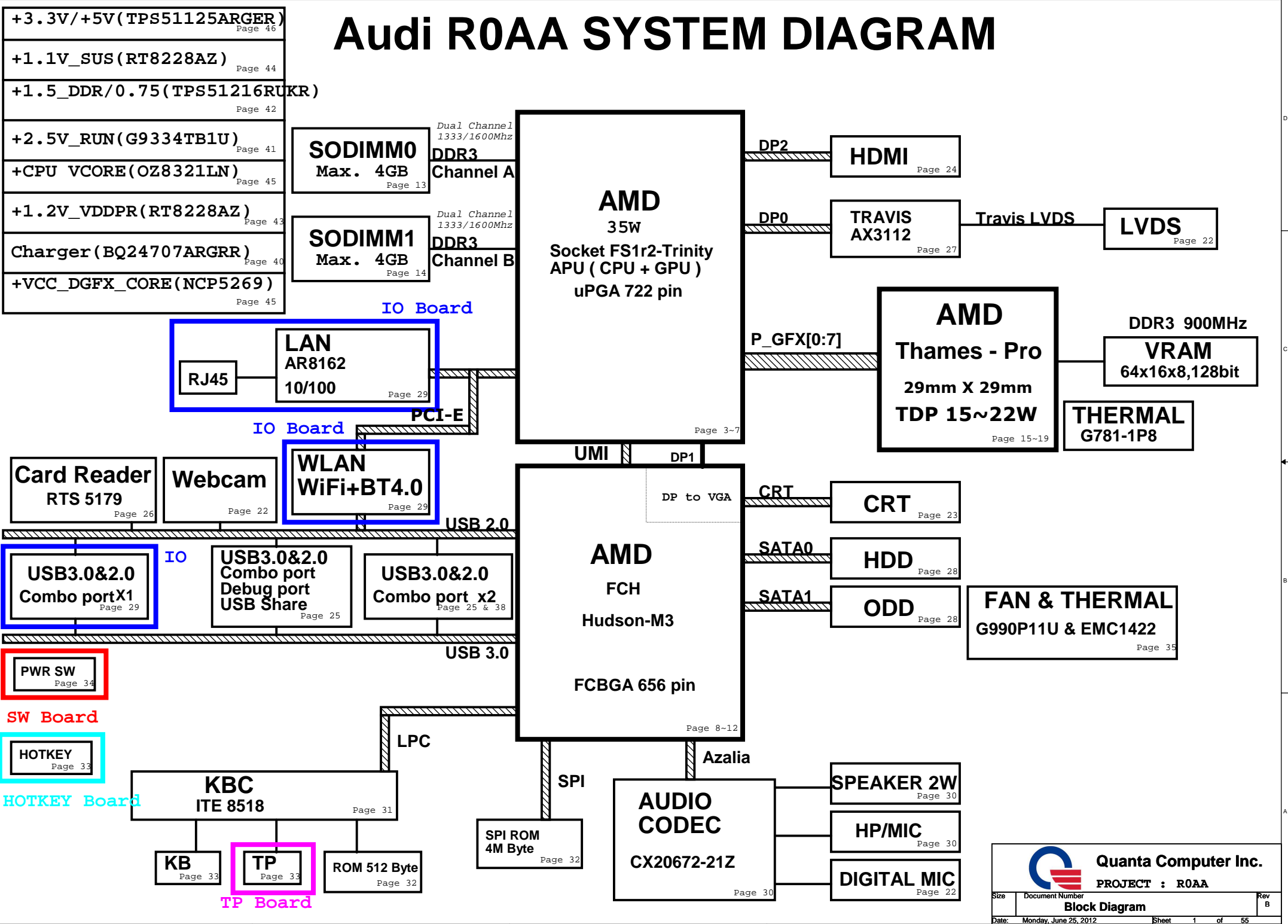


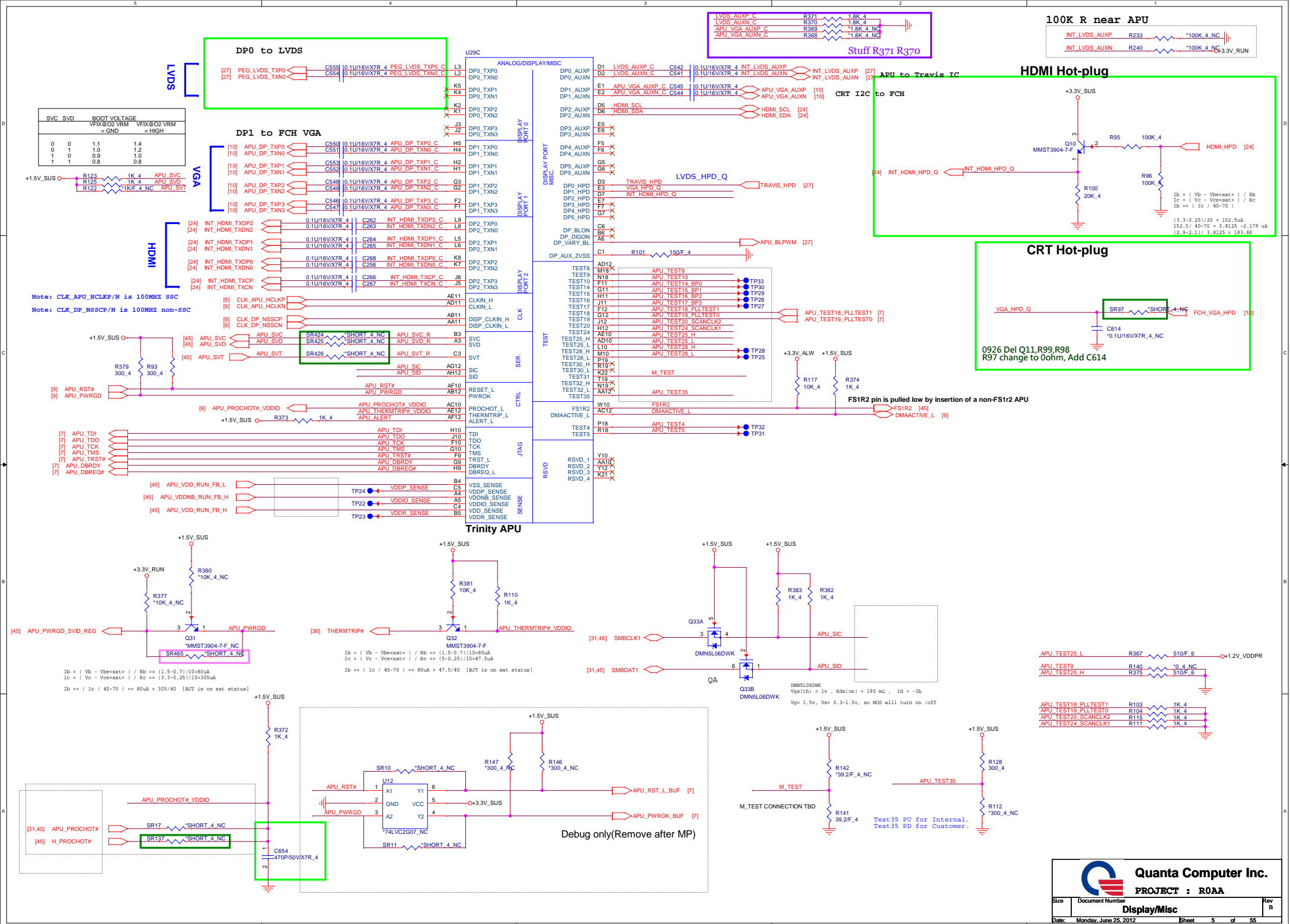
Audi R0AA SYSTEM DIAGRAM



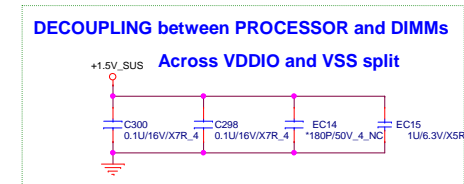
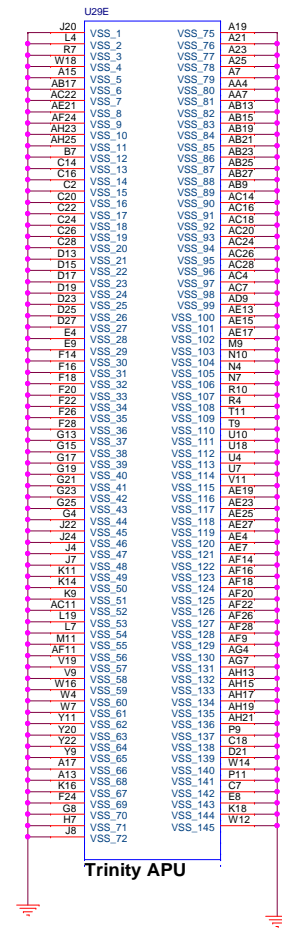
USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC

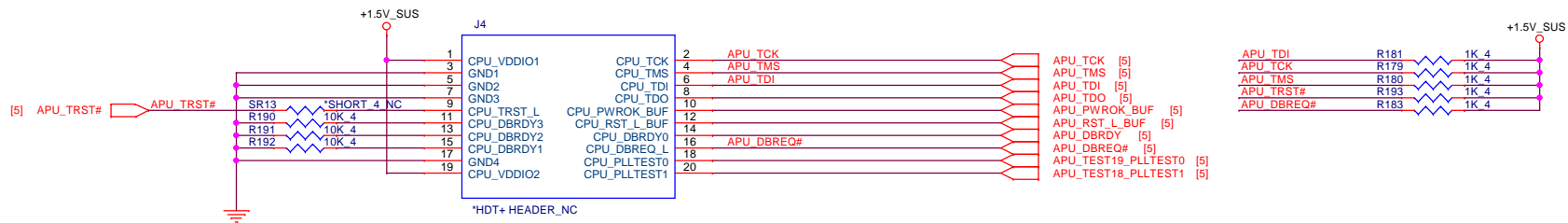


PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



HDT+ Connector

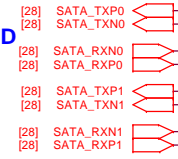
Debug only
Remove after MP



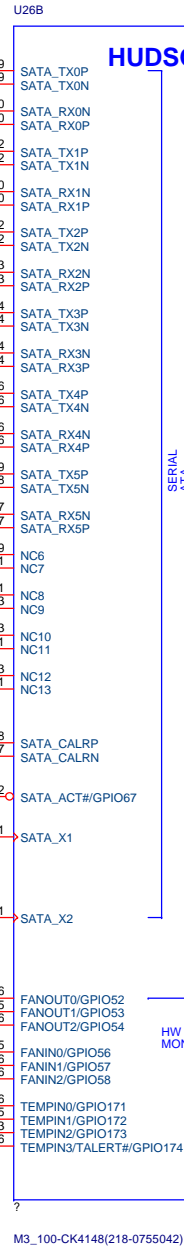
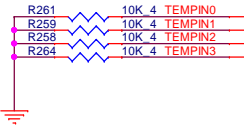
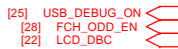
Quanta Computer Inc.
PROJECT : R0AA

SATA HDD/SSD

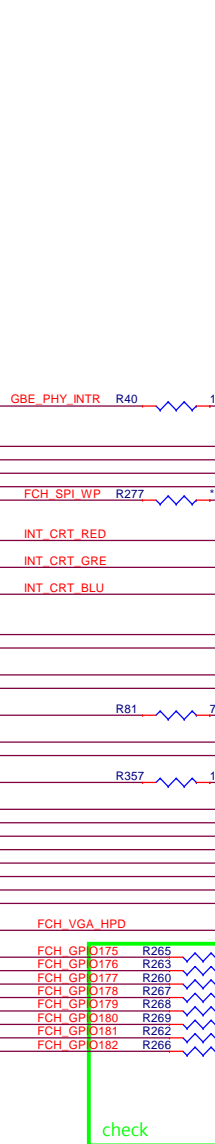
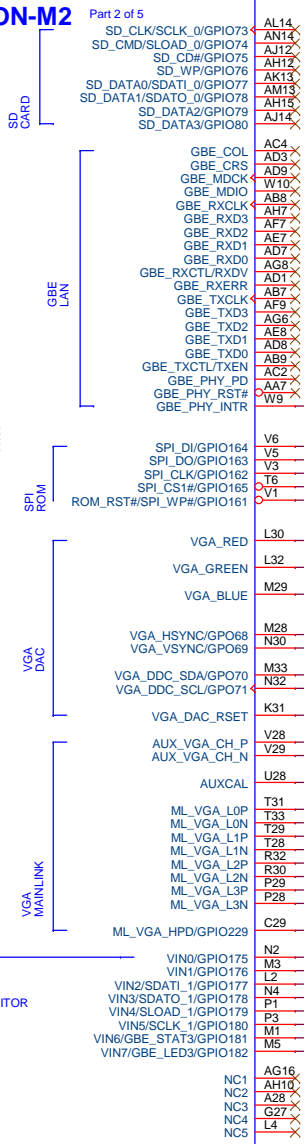
SATA ODD



Integrated Clock Mode:
Leave unconnected.

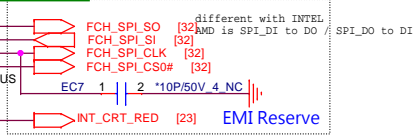
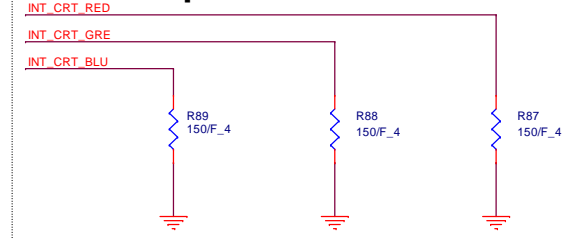


HUDSON-M2



check

R place close to FCH

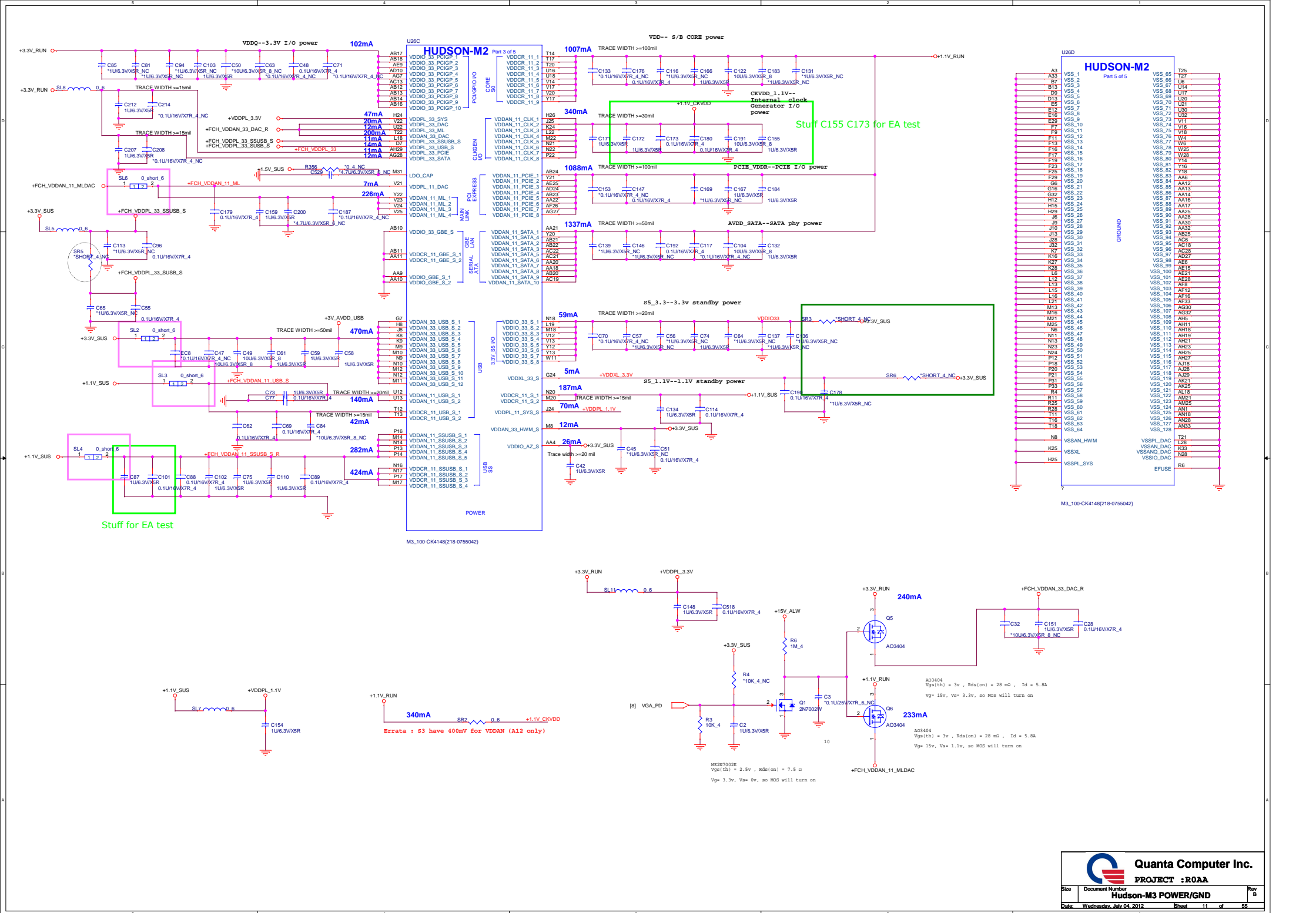


EMI Reserve

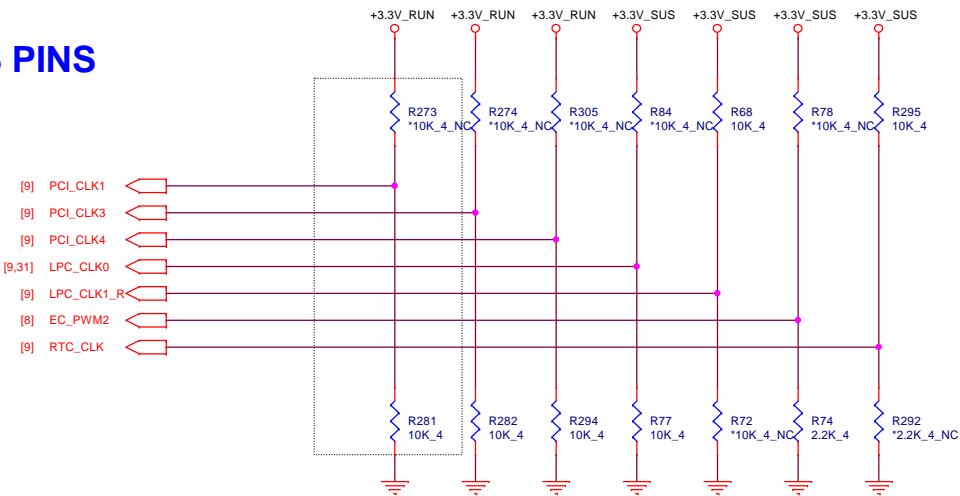
FCH_VGA_HPDP [5]



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STRAPS PINS

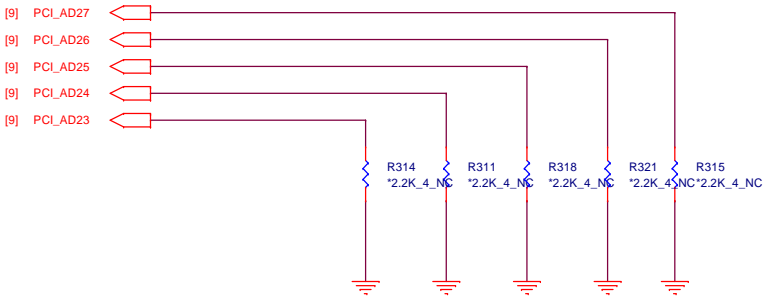


REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED Setting	LPC ROM	S5 PLUS MODE DISABLED Setting
PULL LOW	-----	FORCE PCIe Gen1 Setting	-----	IGNORE DEBUG STRAP Setting	FUSION CLOCK MODE Setting	EC DISABLED Setting	CLKGEN DISABLED	SPI ROM Setting	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

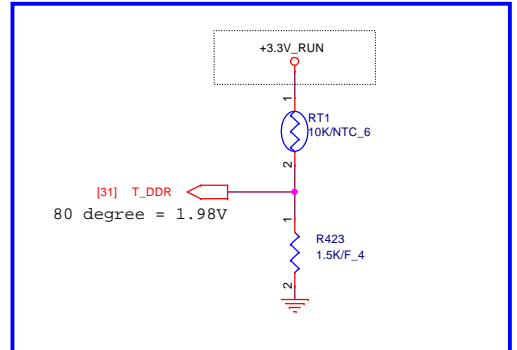
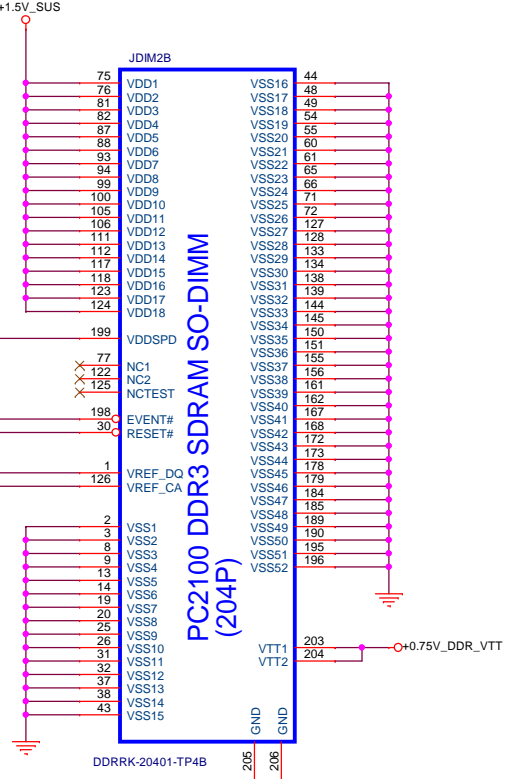
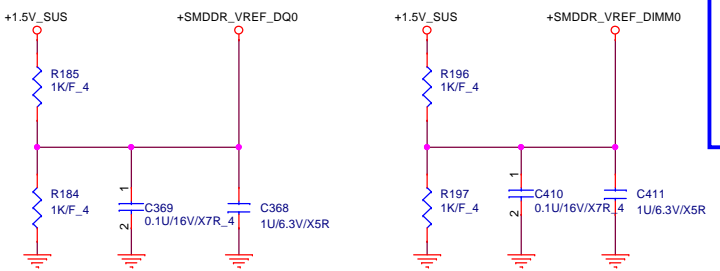
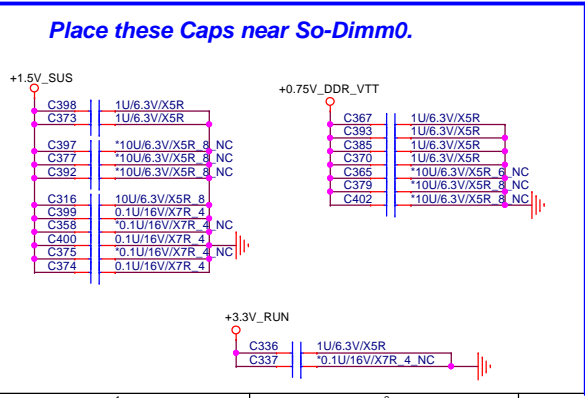
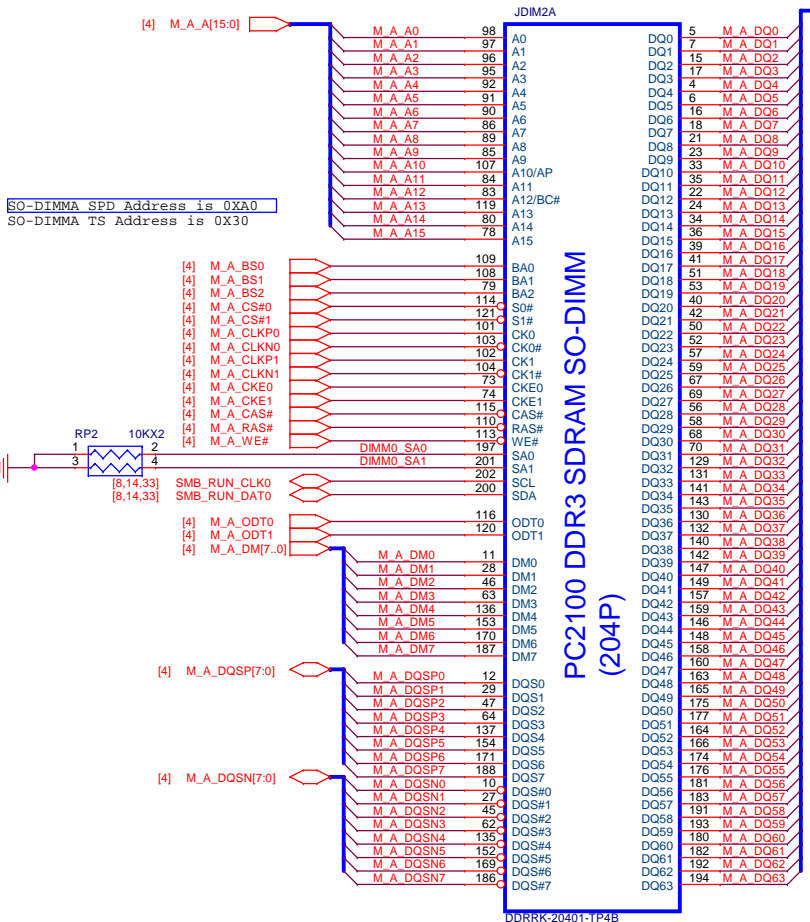


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL Setting	DISABLE ILA AUTORUN Setting	USE FC PLL Setting	USE DEFAULT PCIe STRAPS Setting	DISABLE PCI MEM BOOT Setting
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

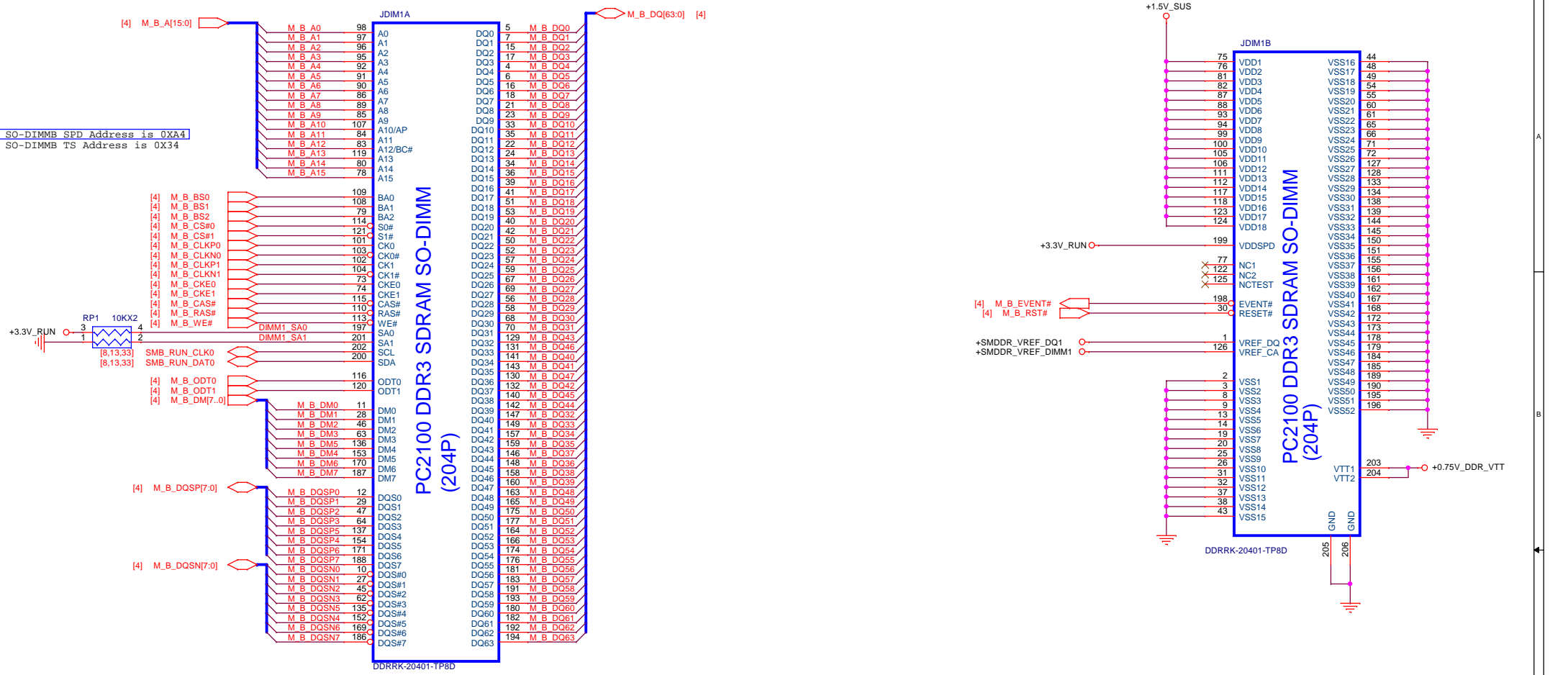


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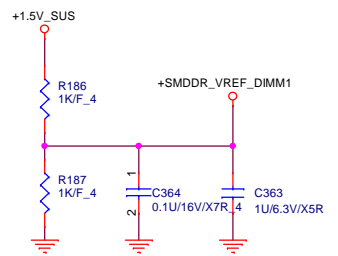
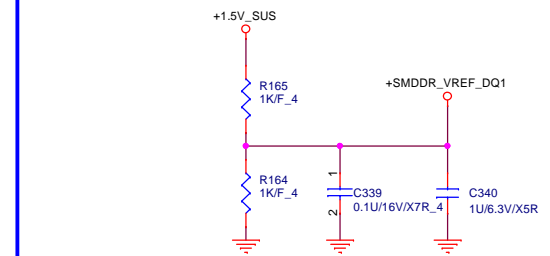
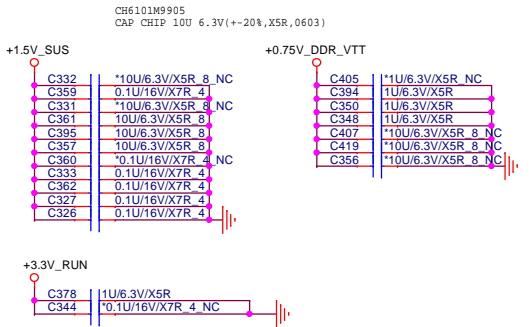
PROJECT : R0AA

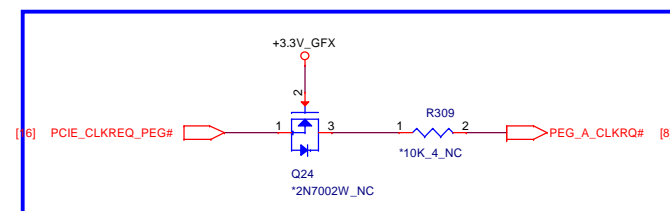
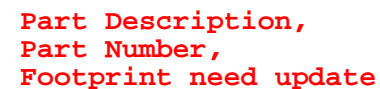


SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



Place these Caps near So-Dimm1.

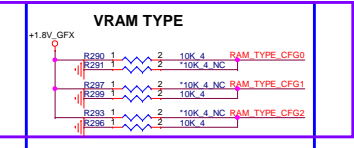
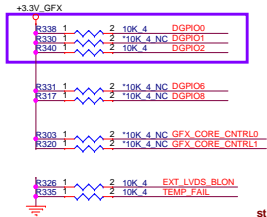




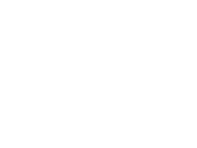
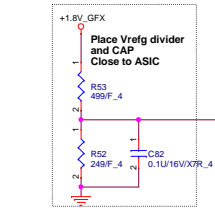
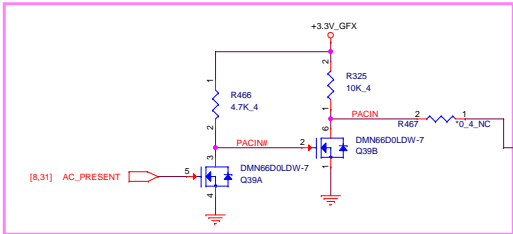
Support Themas & Seymour only

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN3_EN_A	GPIO2	PCIE Gen2 Enable 0 = GEN2 not supported at power-on 1 = GEN2 supported at power-on	1
BIF_VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: VGA Controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAHSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
CEC_DIS	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0 = Disable ; 1 = Enable	0
RESERVED RESERVED RESERVED RESERVED	GENLK_CLK GPIO8 GPIO21 GENERIC	Allow for Pull-up PADS for the reserved straps but do not install resistor if these GPIOs are used, they must keep low and not conflict during reset	

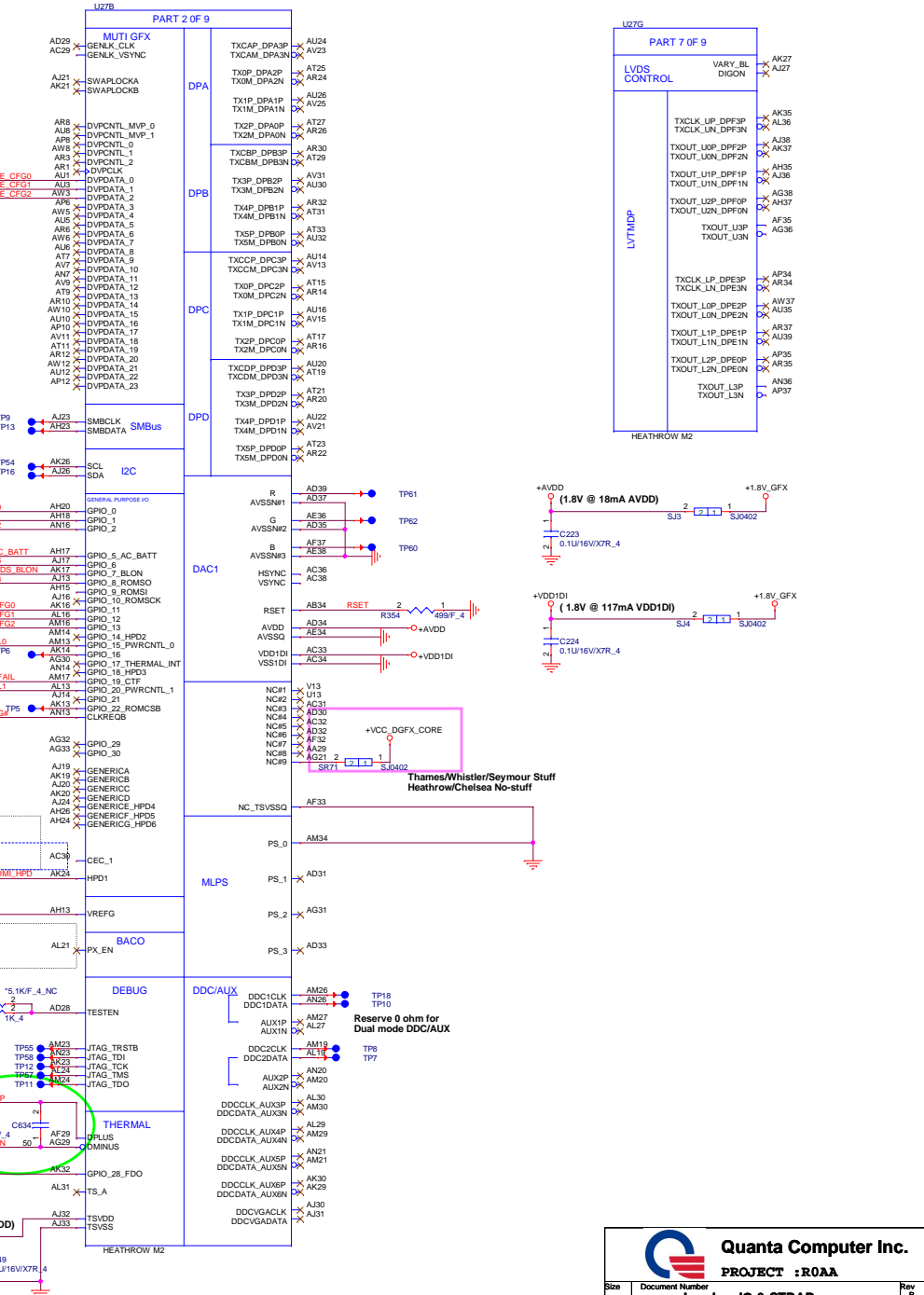
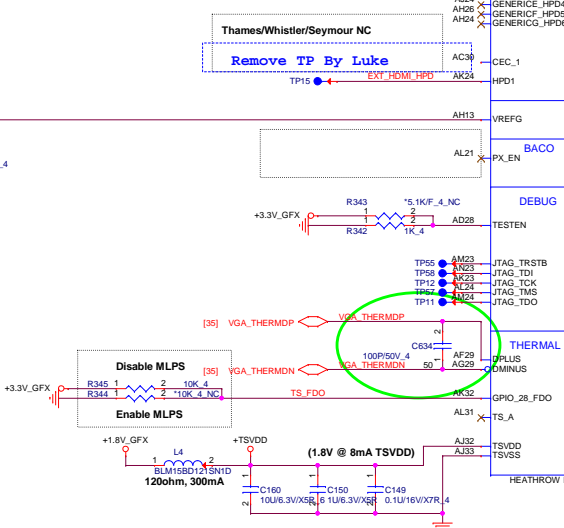
APERTURE SIZE				
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11	
128MB	0	0	0	
256MB	0	0	1	
64MB	0	1	0	



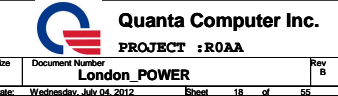
Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5EGGT509	K4W1G1646G-BCL1	For Thames
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZW7W07	H5TQ1G63DFR-11C	For Thames
900MHz Micron 1GB(64M*16*8pcs)	1	0	0	AKD5EGSTL01	MT41J64M16JT	For Thames



Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5EGGT509	K4W1G1646G-BCL1	For Thames
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZW7W07	H5TQ1G63DFR-11C	For Thames
900MHz Micron 1GB(64M*16*8pcs)	1	0	0	AKD5EGSTL01	MT41J64M16JT	For Thames




```
Chelsea uninstall
Thames install,
total 440mA
```




```
[17] VMA_MA[13..0]
[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]
```

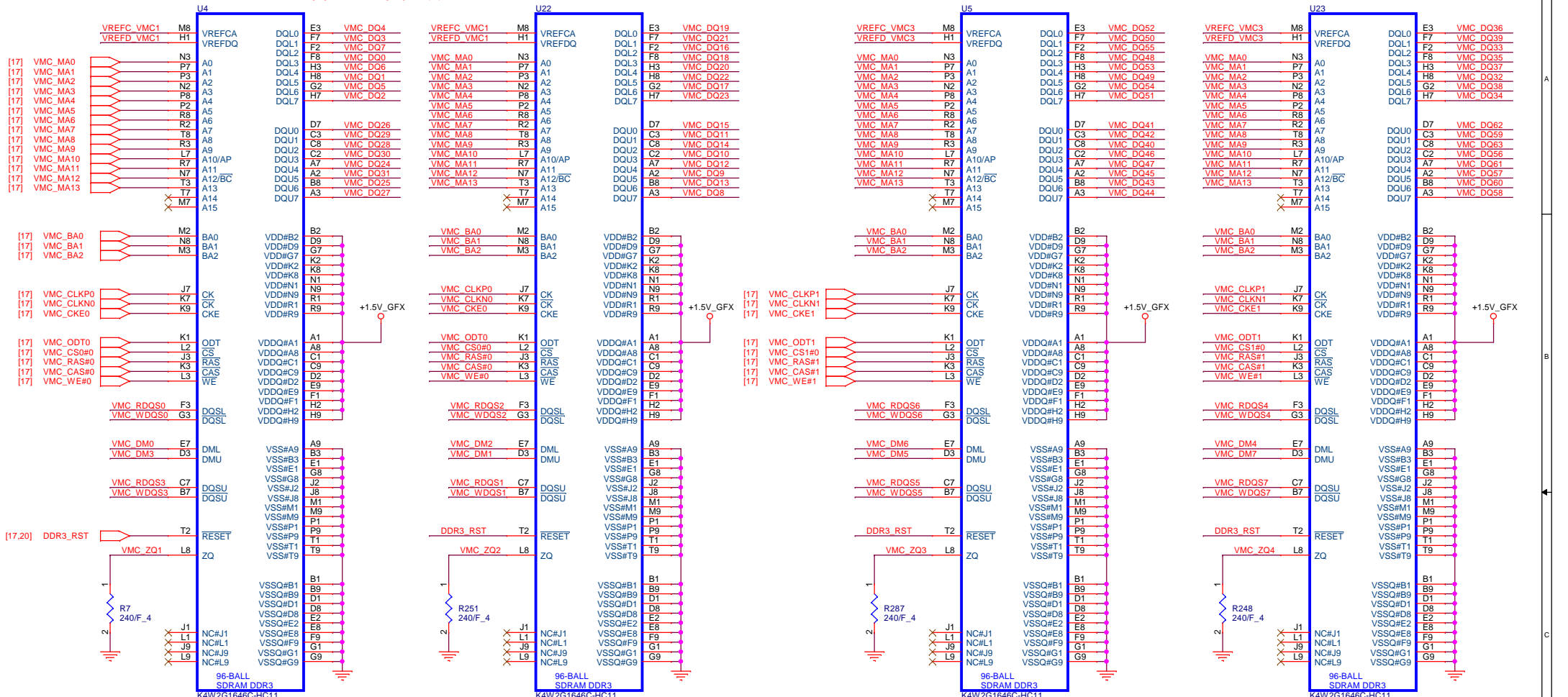


Quanta Computer Inc.
PROJECT : R0AA

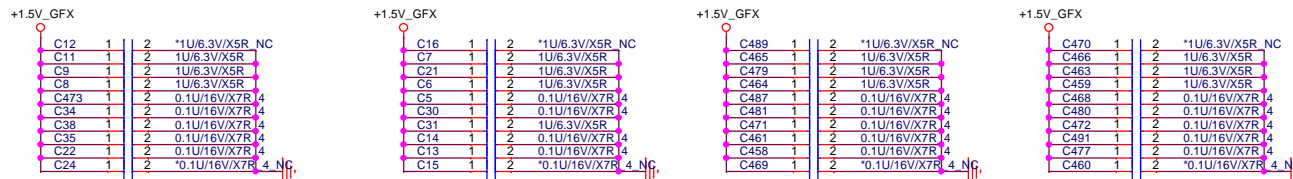
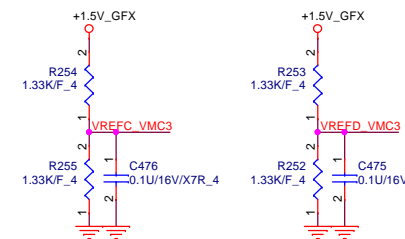
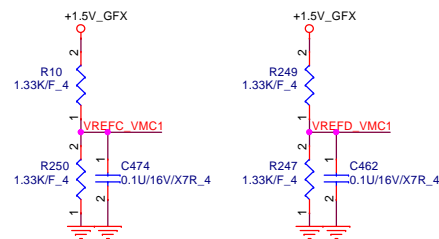
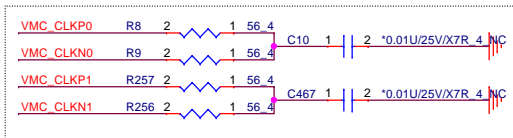
Size	Document Number	Rev
	N11M-GE2 VRAM-1(DDR3 BGA96)	1A
Date:	Friday, June 29, 2012	Sheet 20 of 55

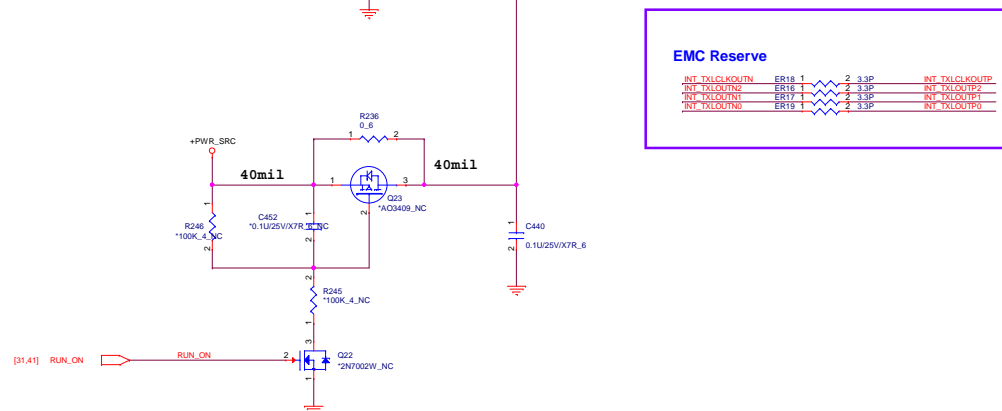
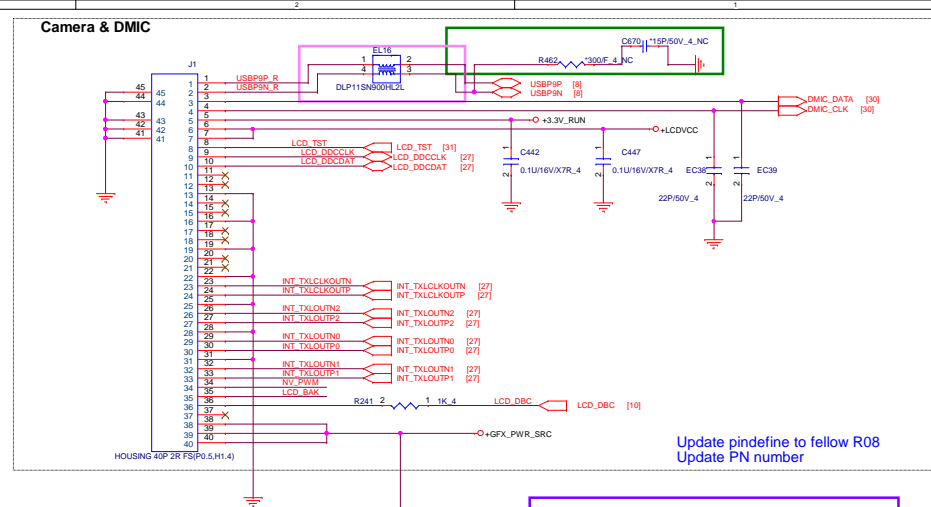
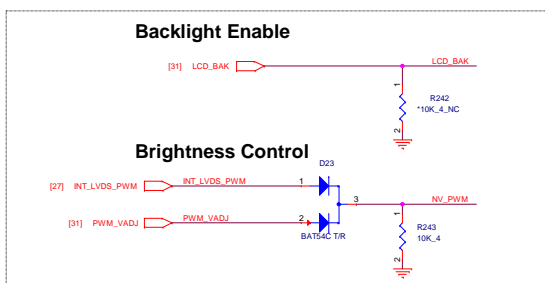
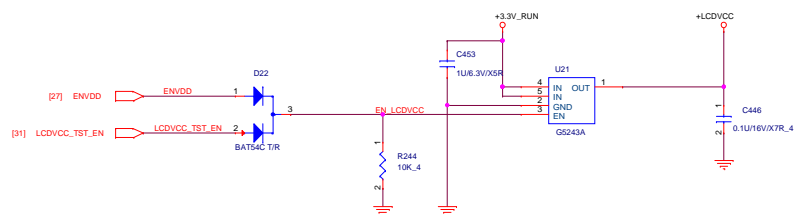
CHANNEL B: 1024MB DDR3

[17] VMC_MA[13..0]
[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

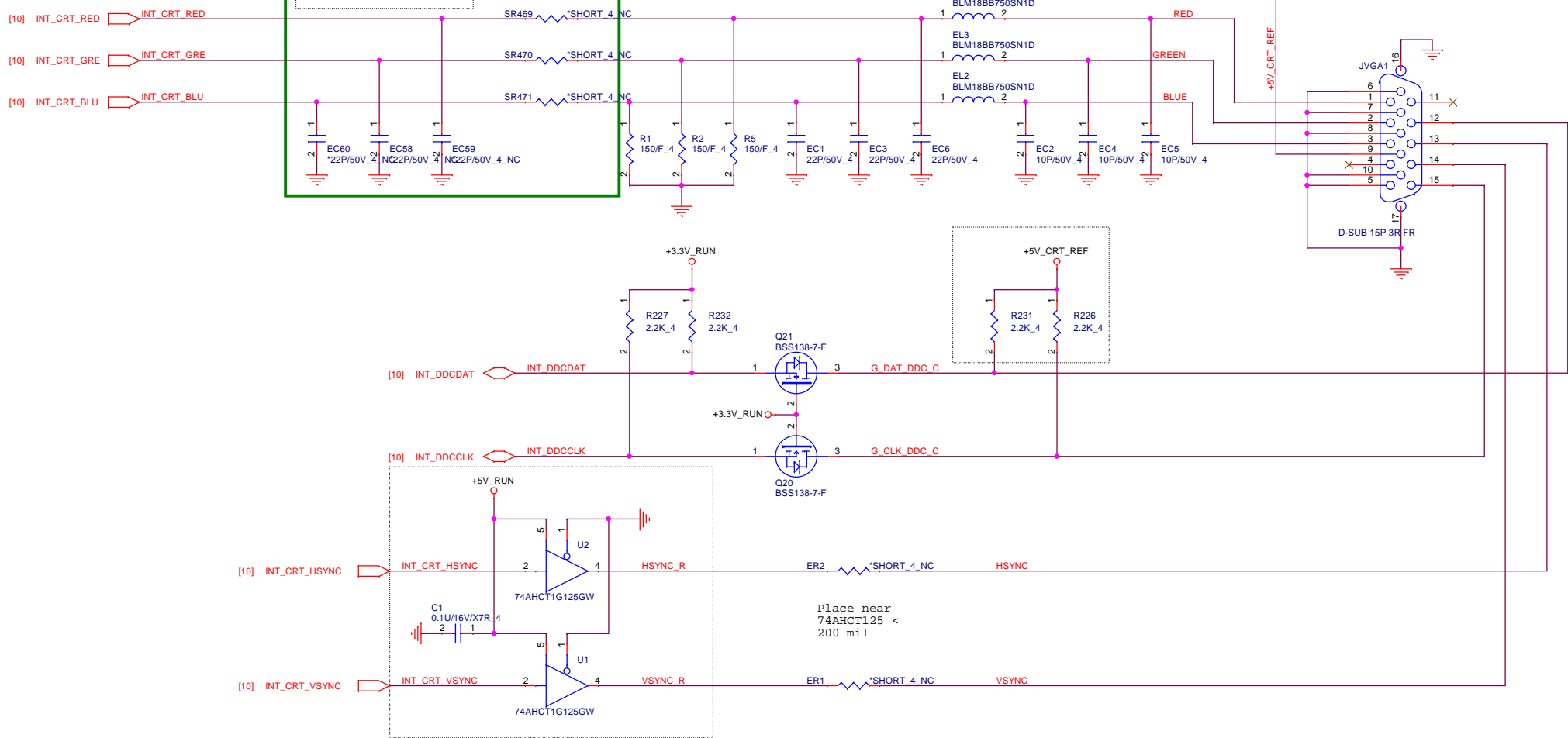


Placement has to be close to VRAM

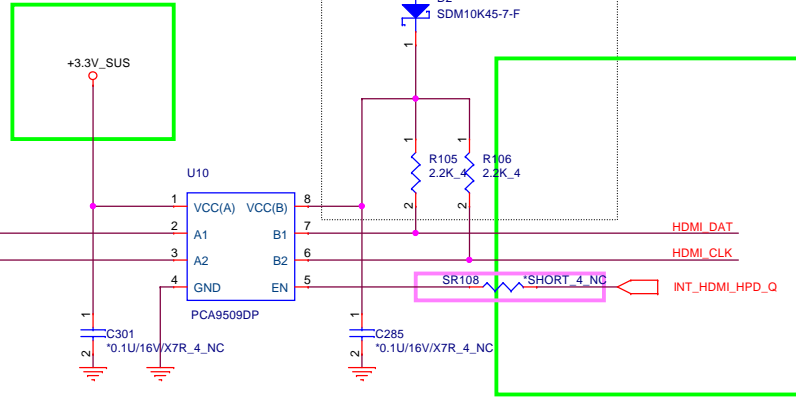




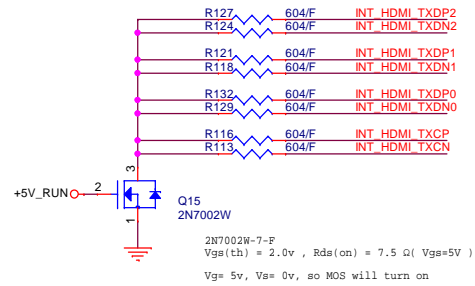
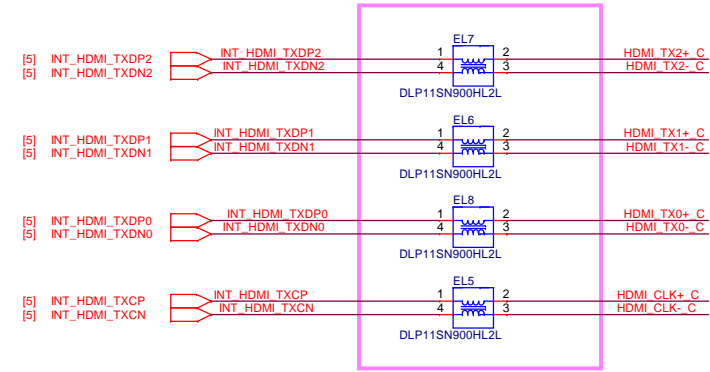
Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



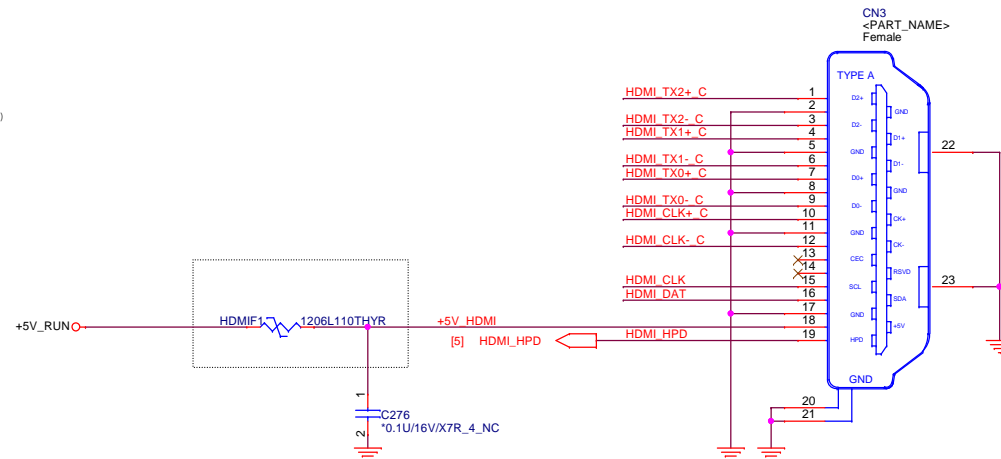
0926 Change 1.5VS to 3.3VS



Reserve for EMI and close to HDMI CONN



HDMI Conn.



Quanta Computer Inc.

PROJECT : R0AA

S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

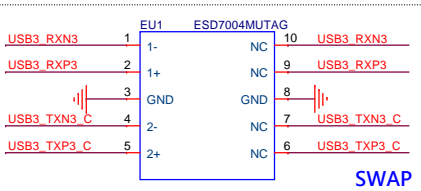
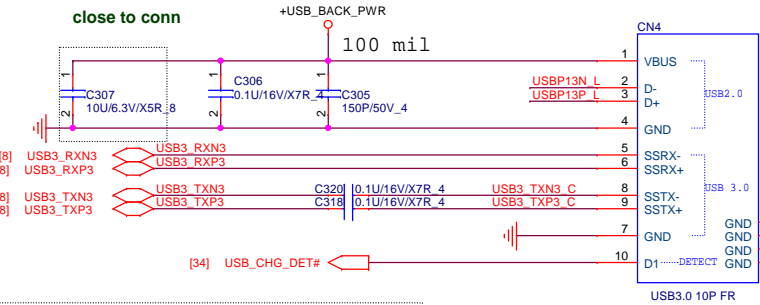
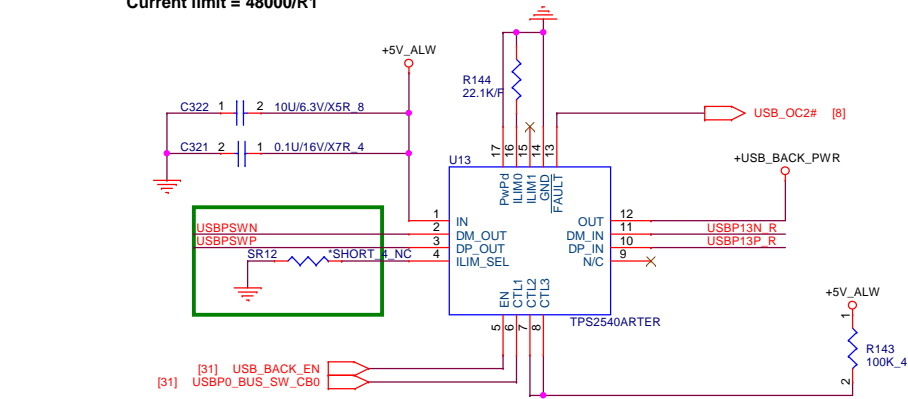
USB Power share

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

OC limitation	R1	mA
	100k ohm	480
	22.1k ohm	2171

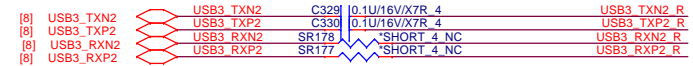
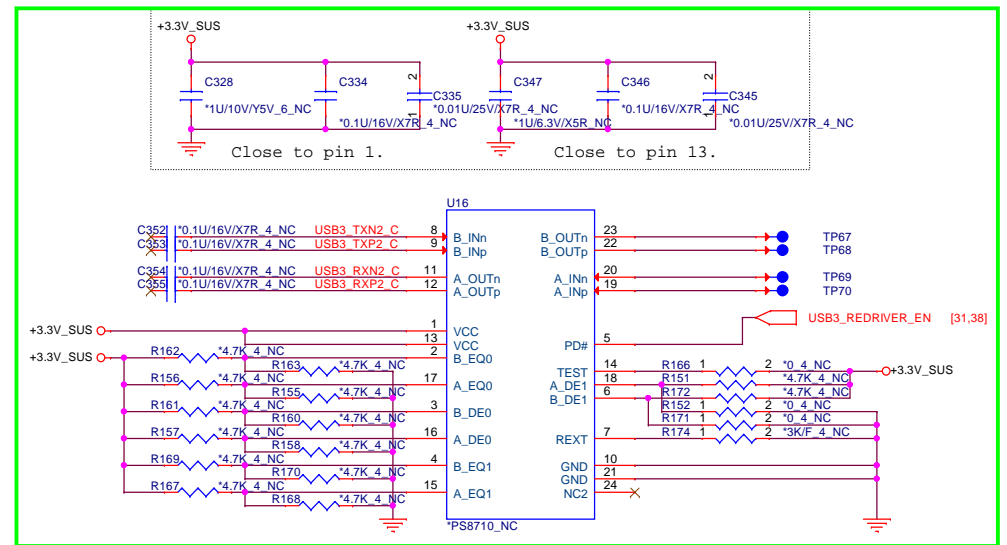
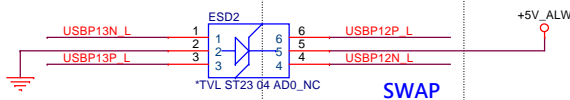
Applied Now

Current limit = 48000/R1

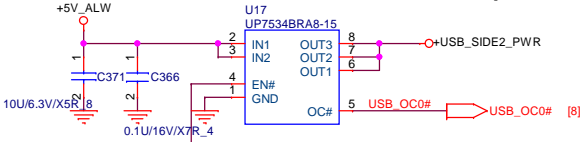


ESD Function

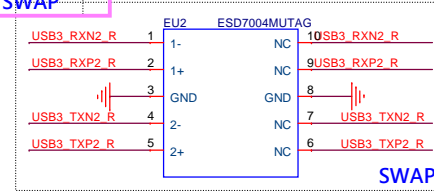
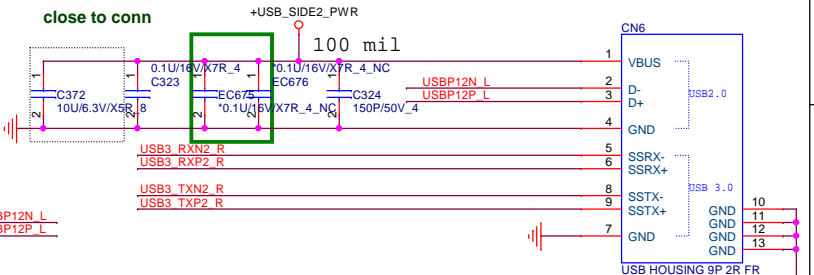
Place ESD diodes as close as USB connector.



I continuous 1.5A OC 2.0A M13 Request



close to conn

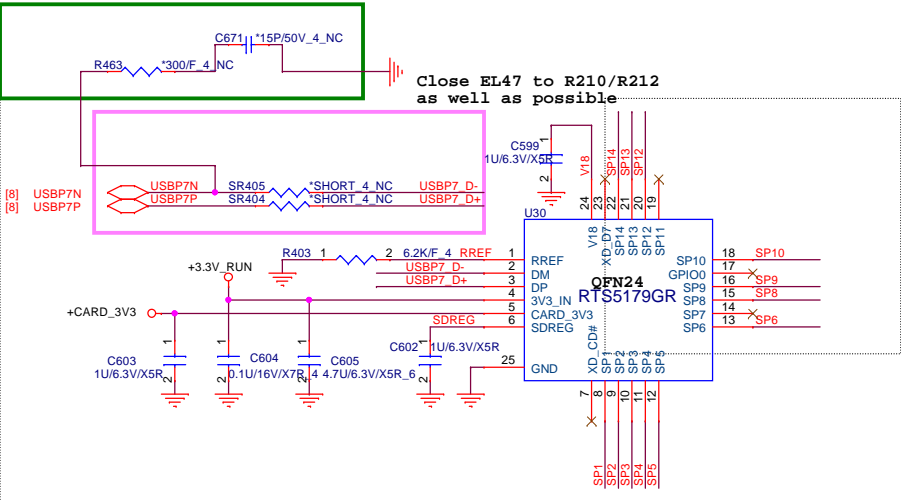
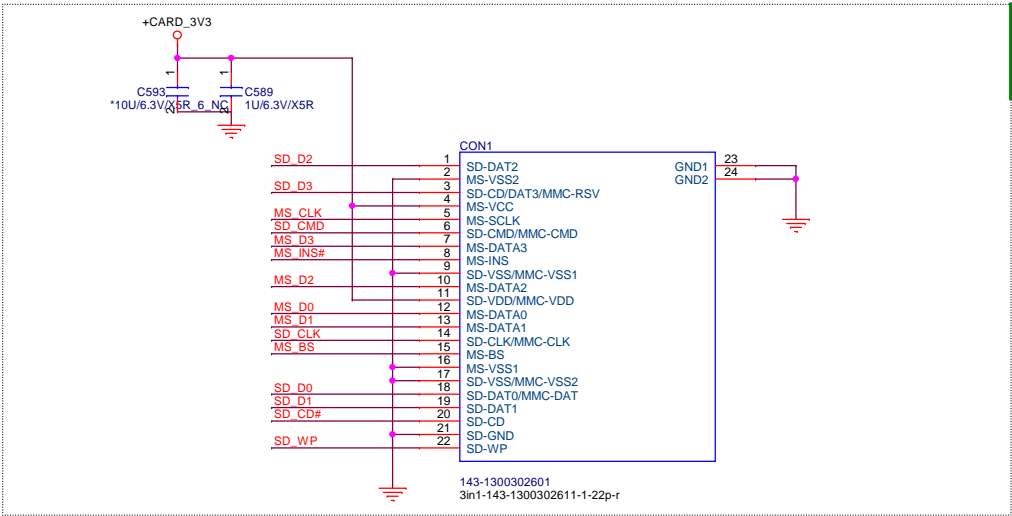


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PROJECT : R0AA

Size	Document Number	Rev
	USB 3.0 port / USB power share	B
Date: Thursday, June 28, 2012	Sheet 25 of 55	

Cardreader (RTS5179GR) Support SD3.0 USH50

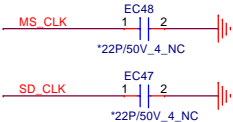
Change CON1 footprint to 3in1-143-1300302611-1-22p-r(follow R09)

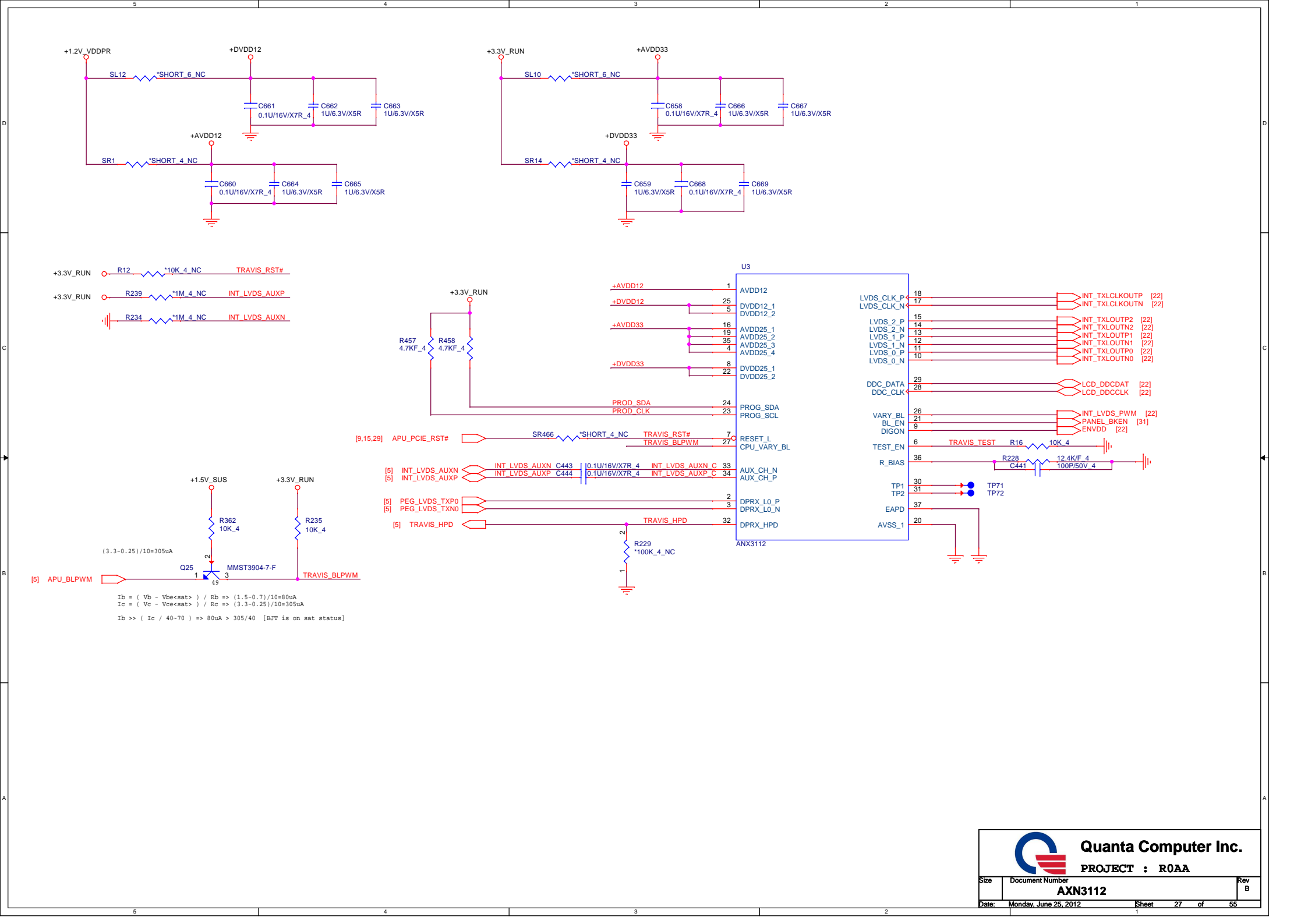


Share Pin

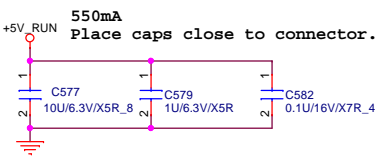
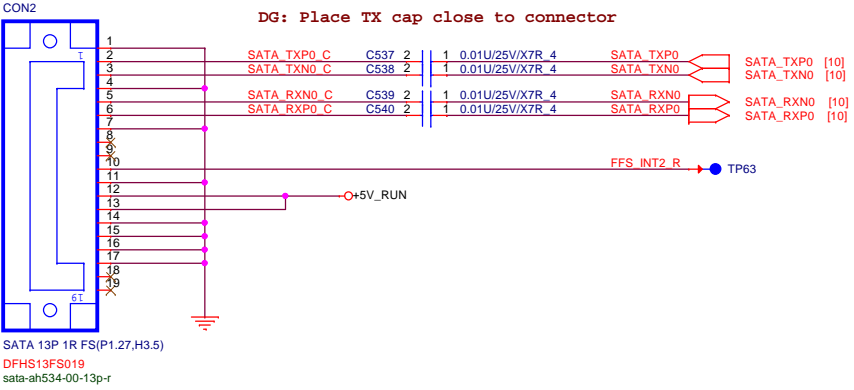
	SD CARD	MS CARD
SP1	SW_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

SP1	SD_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

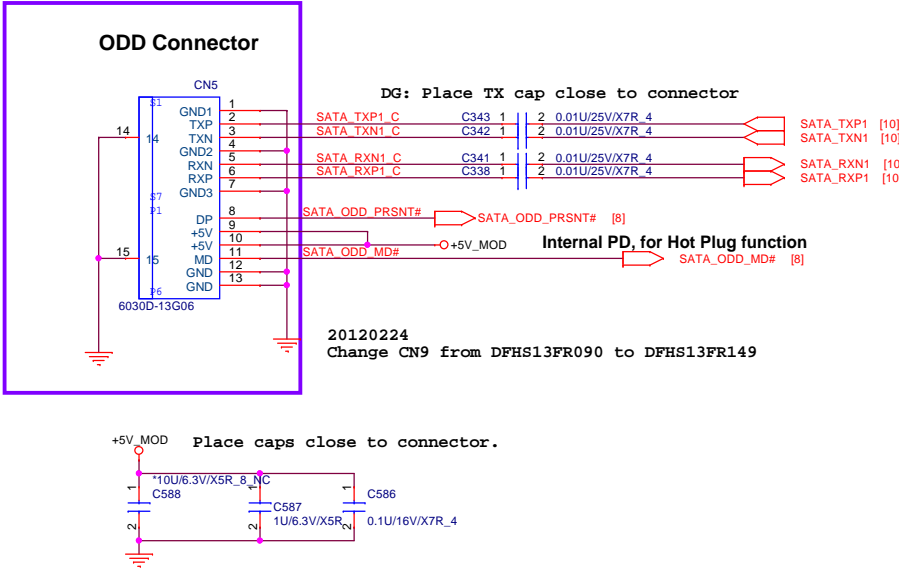




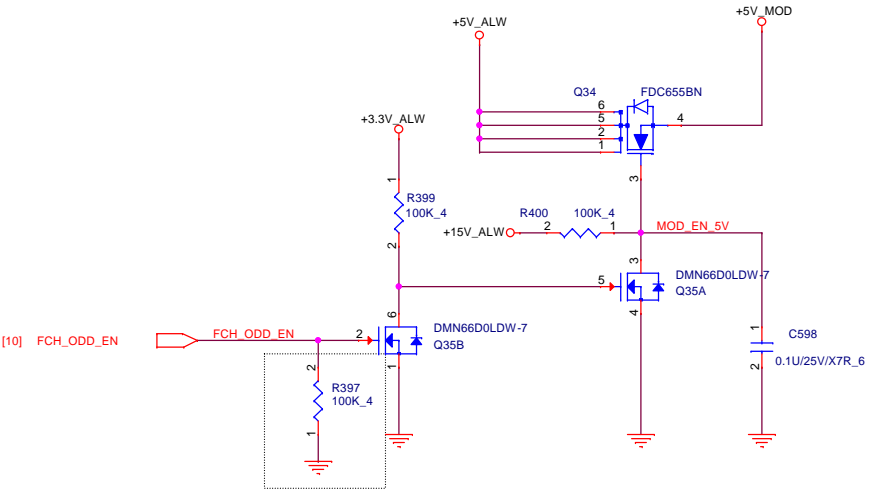
HDD

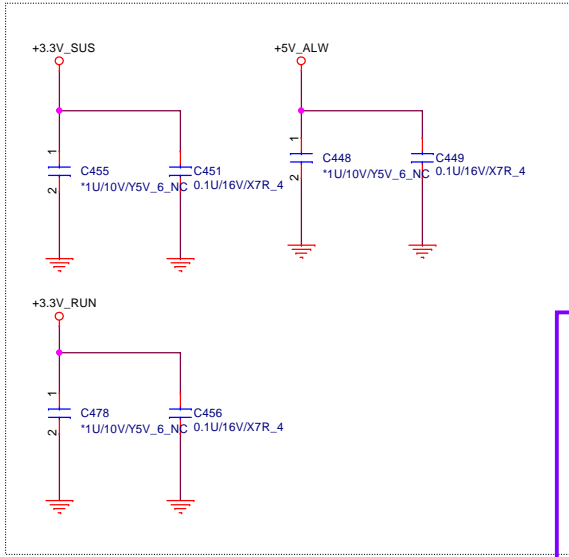


ODD

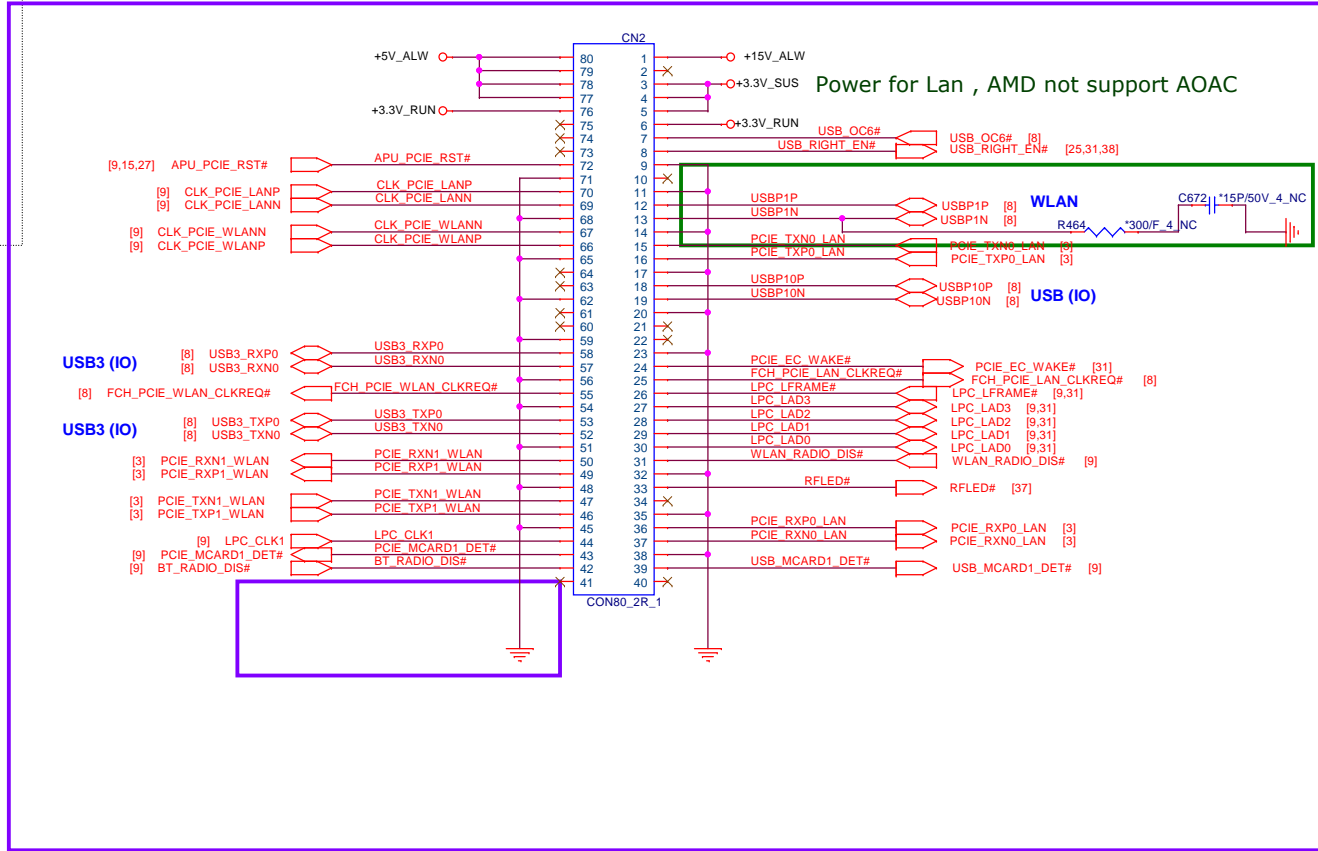


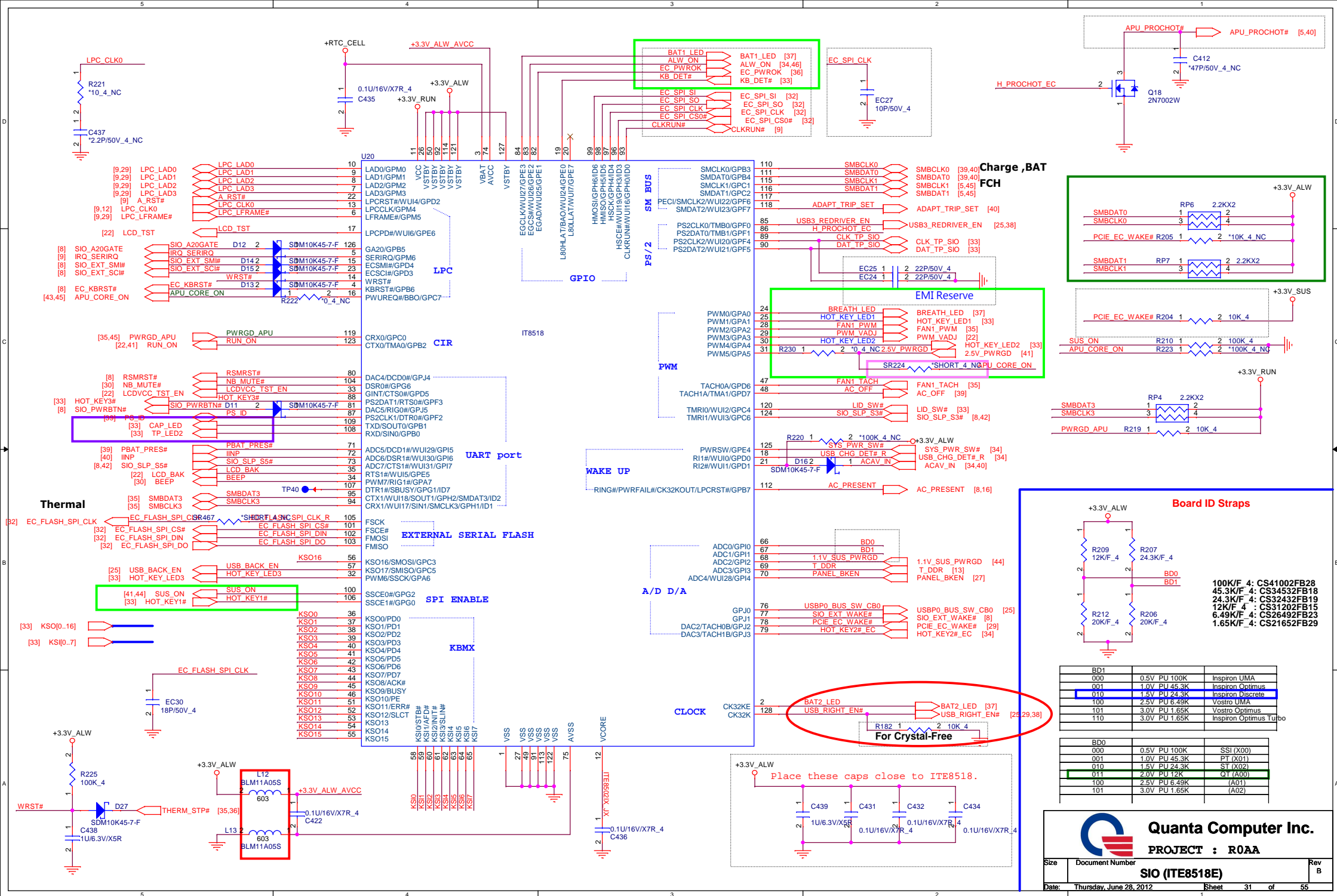
Support Zero power ODD





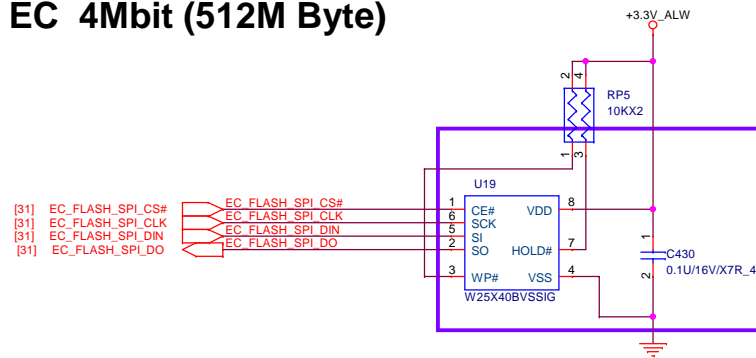
20120229
Change CN9 footprint from "88161-08001-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"



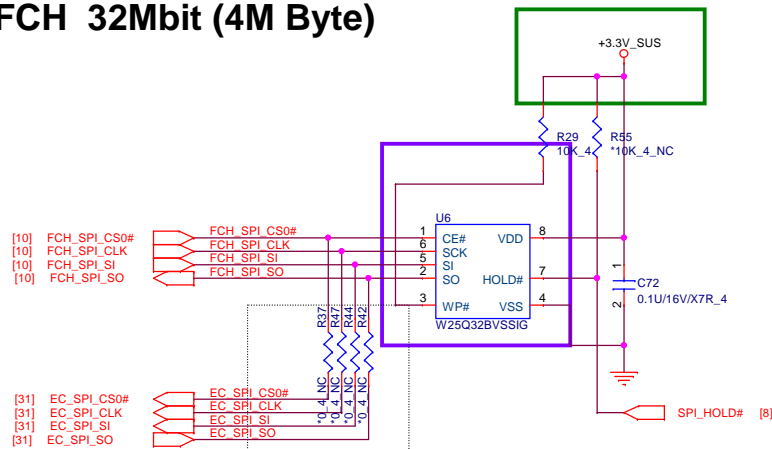


FLASH / RTC

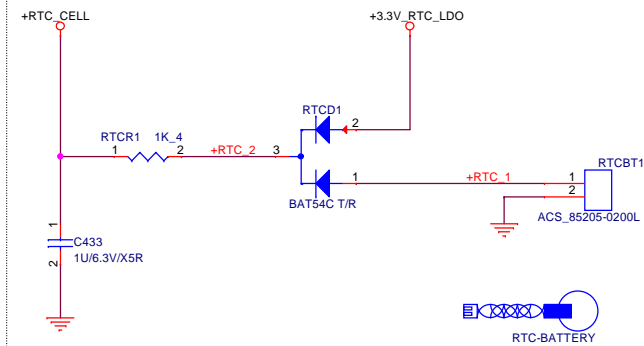
For EC 4Mbit (512M Byte)



For FCH 32Mbit (4M Byte)



RTC



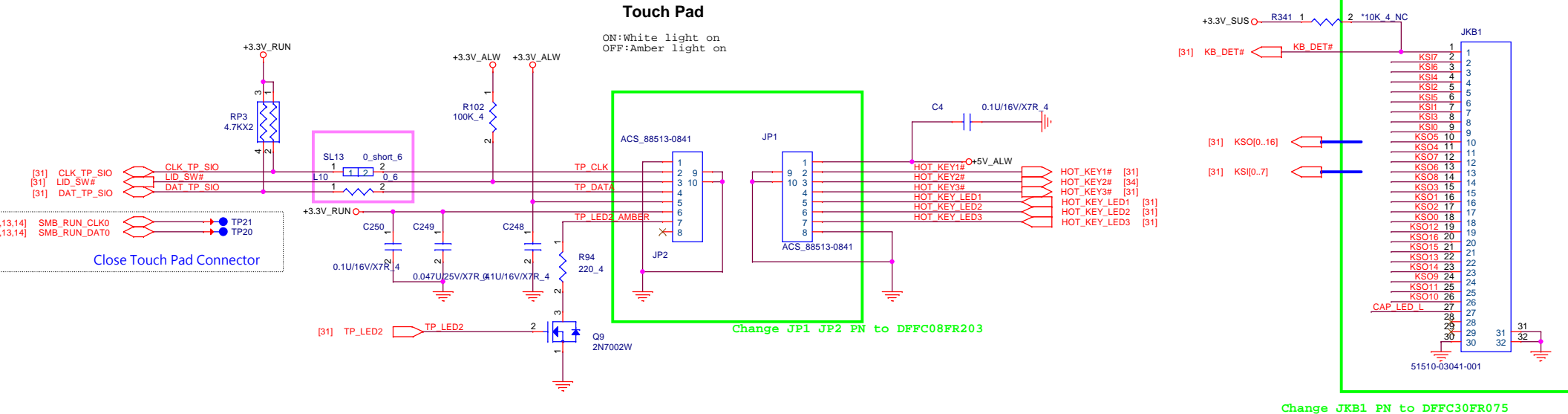
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA



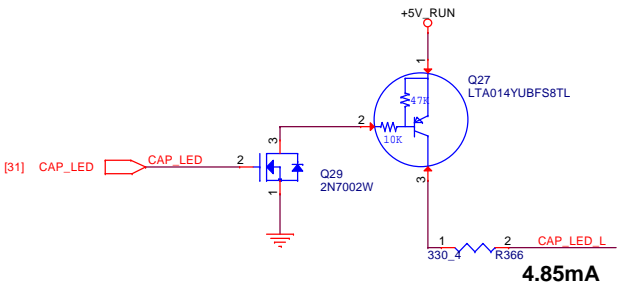
Quanta Computer Inc.

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KEYBOARD CONNECTOR

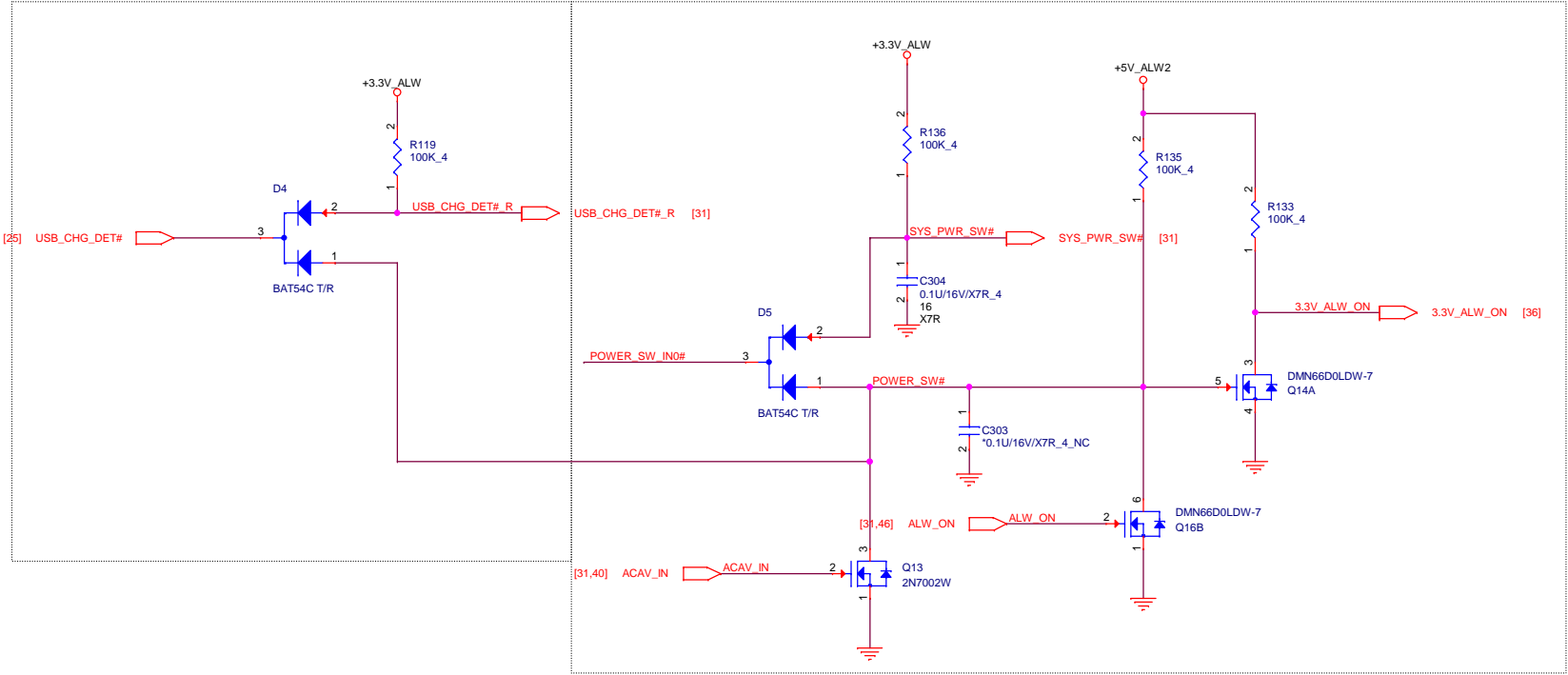


$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



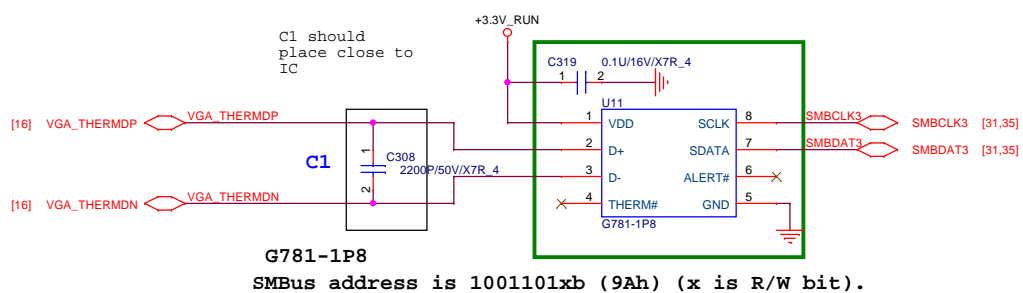
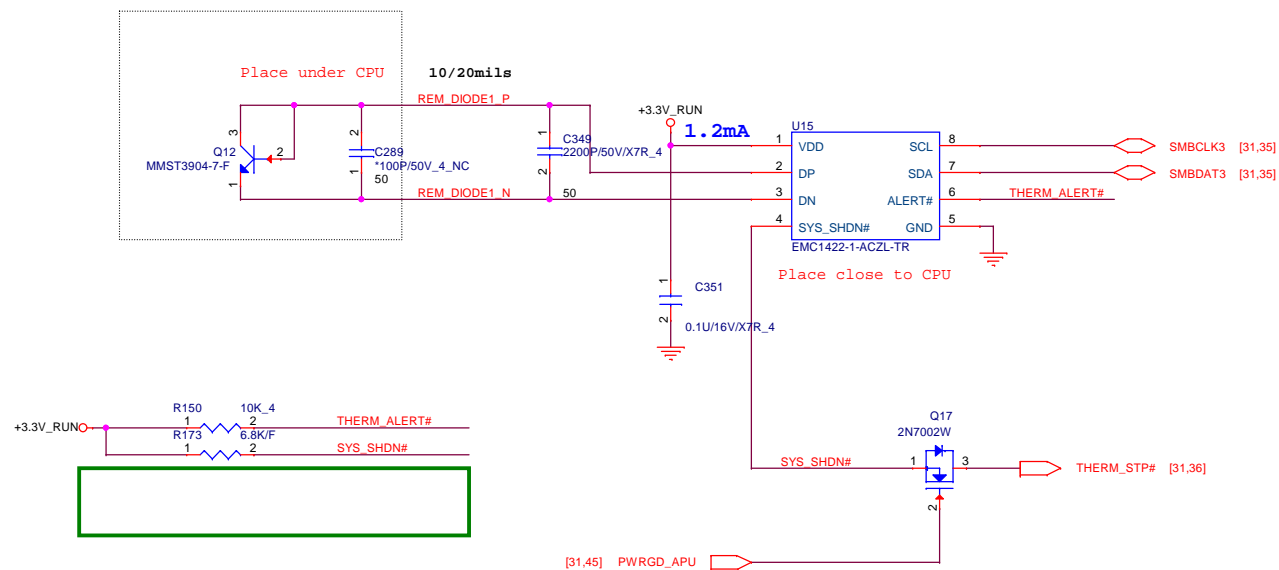
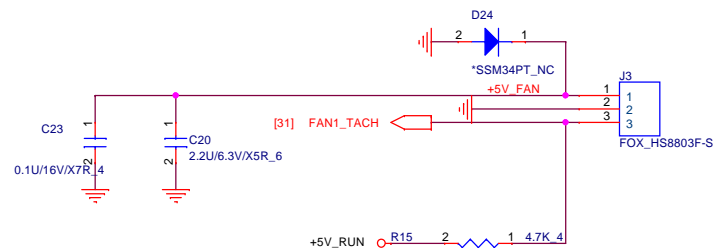
For USB charger usage

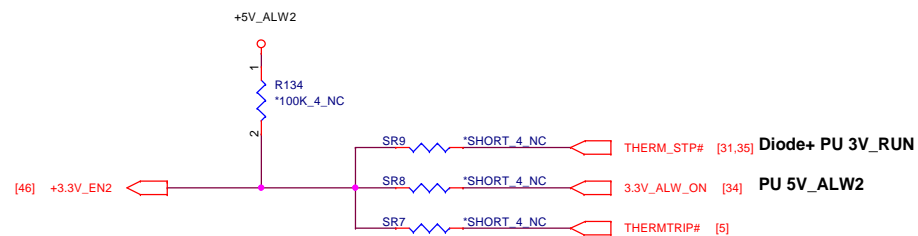
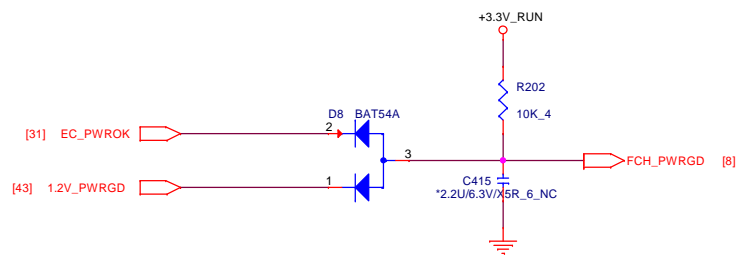
3V ALW ON POWER LOGIC



TO PWR button board





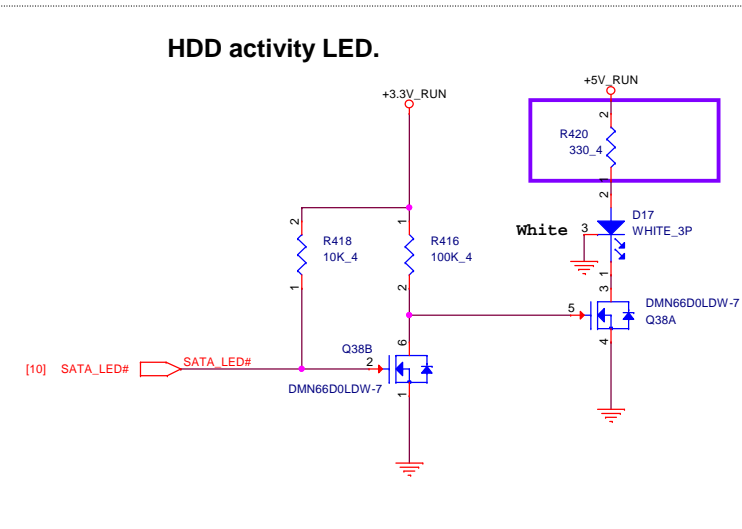
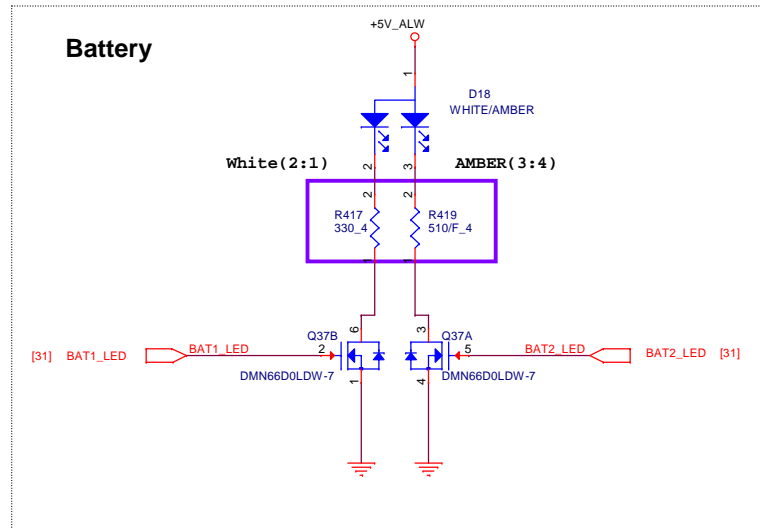
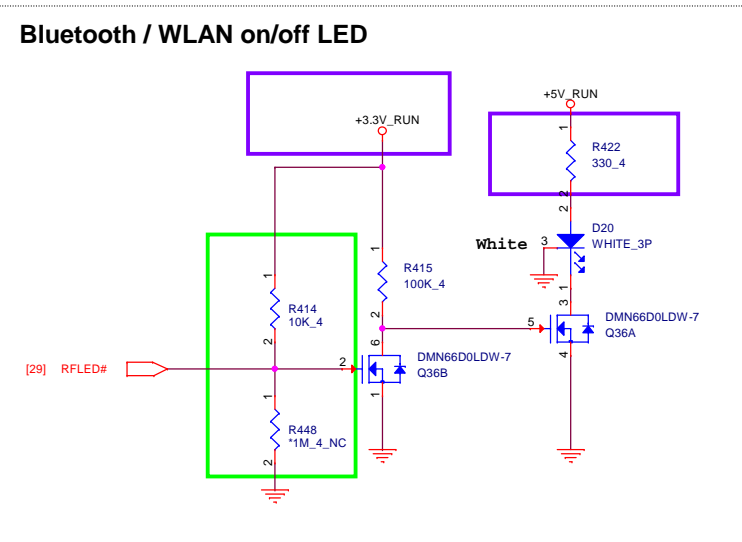
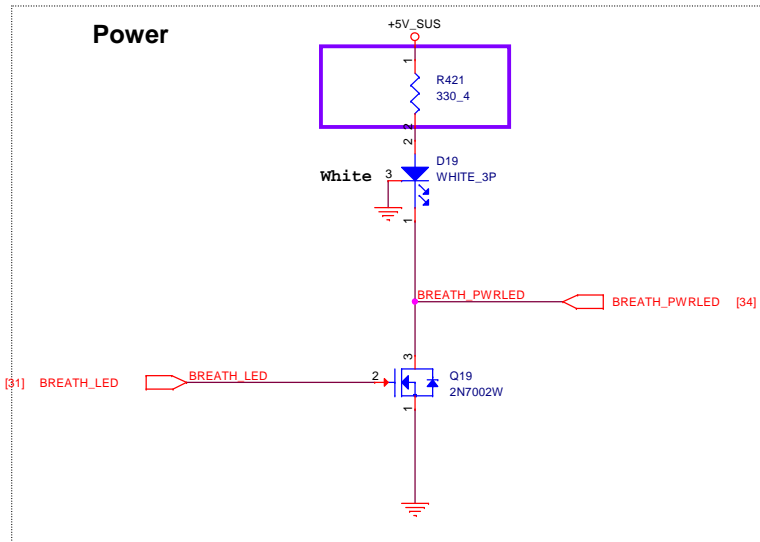


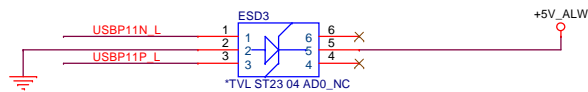
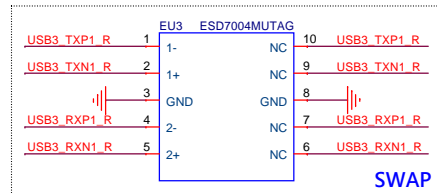
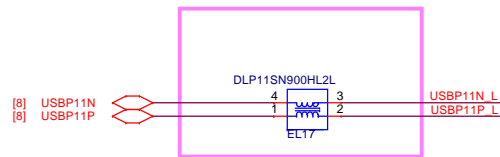
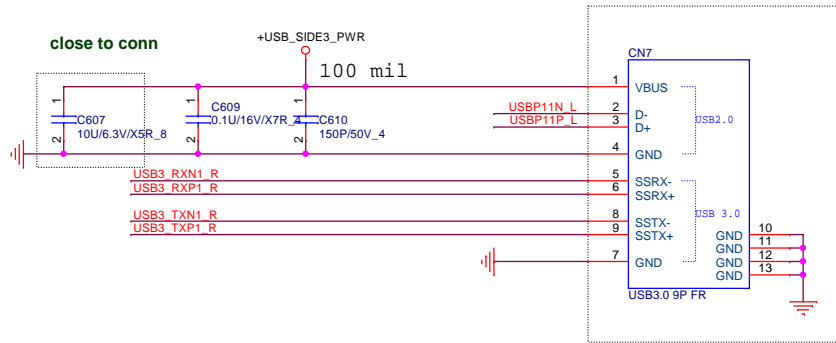
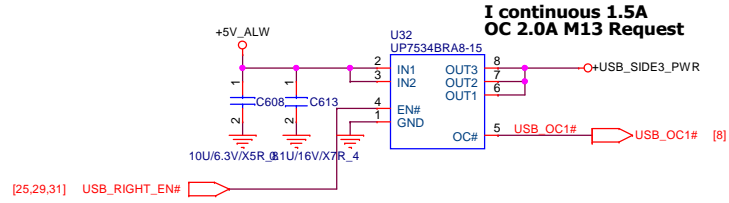
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PROJECT : R07

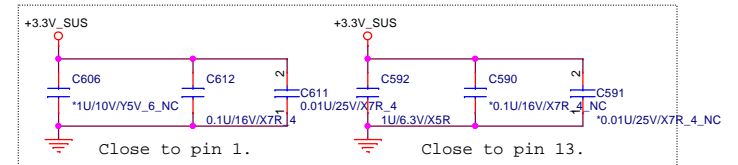
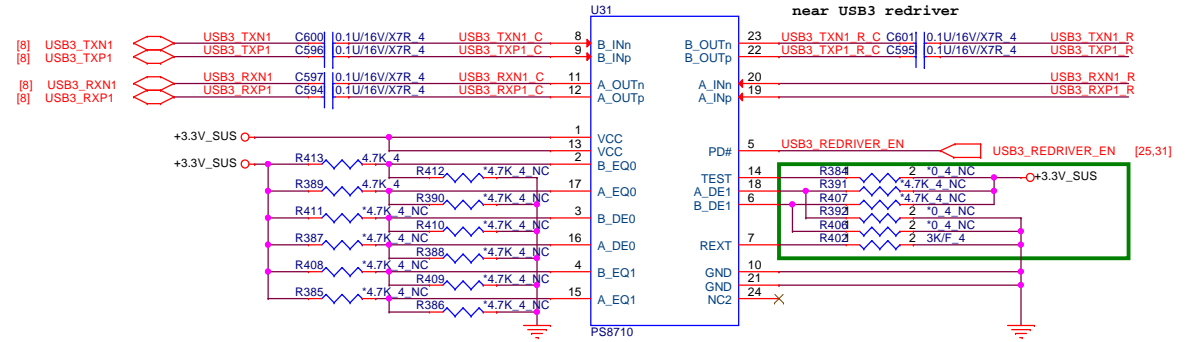
Size	Document Number	Rev
		1A
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System Reset Circuit





Del Colay reserve



Chip test mode enable.
3.3V tolerant. Internally pulled down at ~ 150K ohm
TEST ==
L: Normal operation (default)
H: Test mode enable

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis with boost output swing
HH: 5dB de-emphasis with boost output swing

Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_EQ1, A_EQ0] ==
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_DE1, B_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis with boost output swing
HH: 5dB de-emphasis with boost output swing

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_EQ1, B_EQ0] ==
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

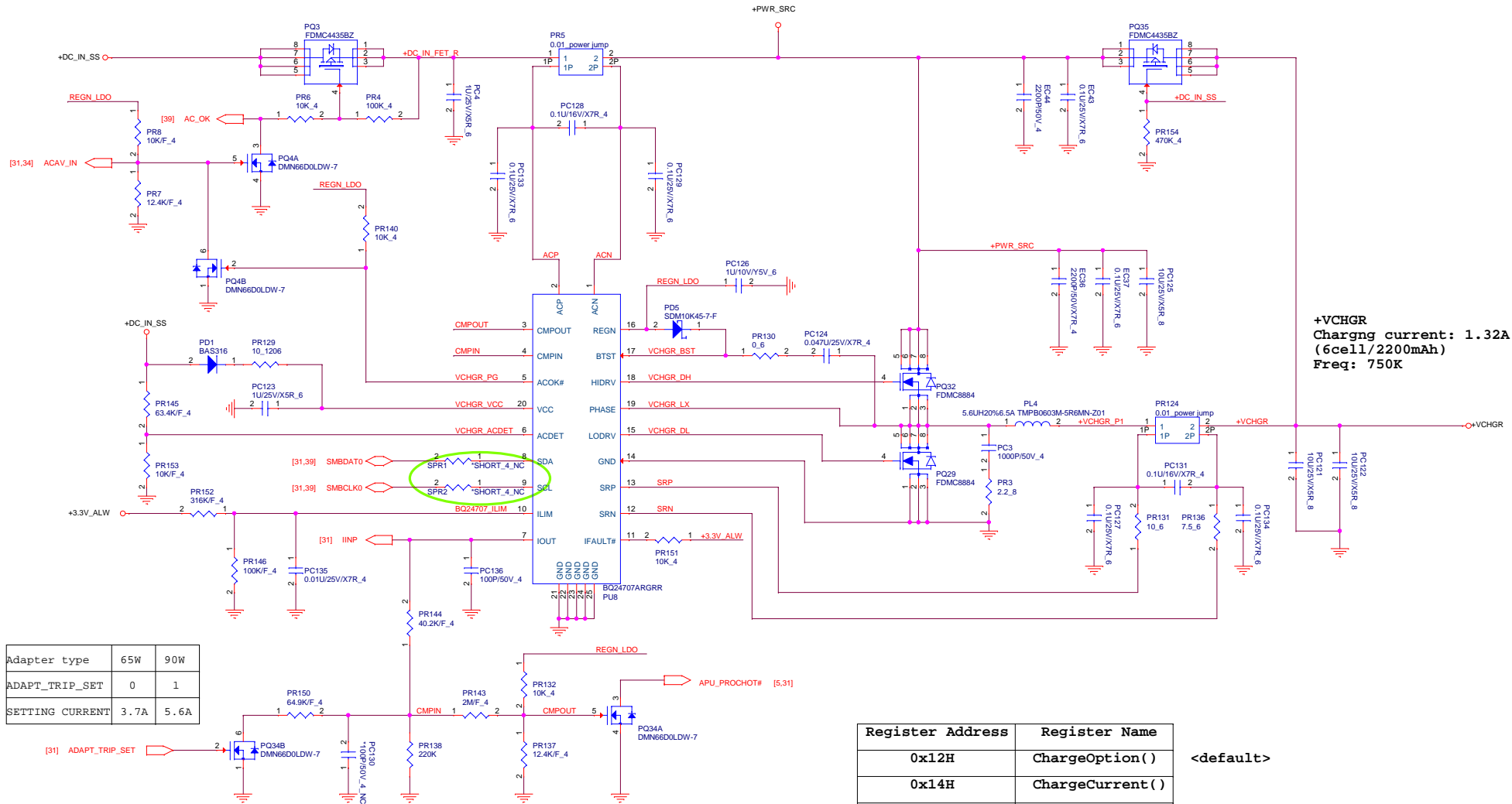


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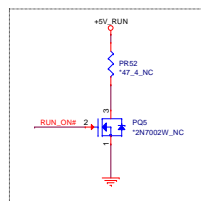
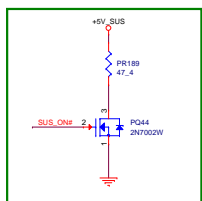
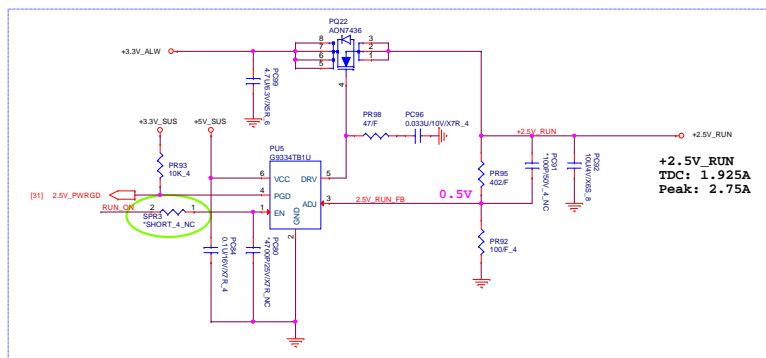
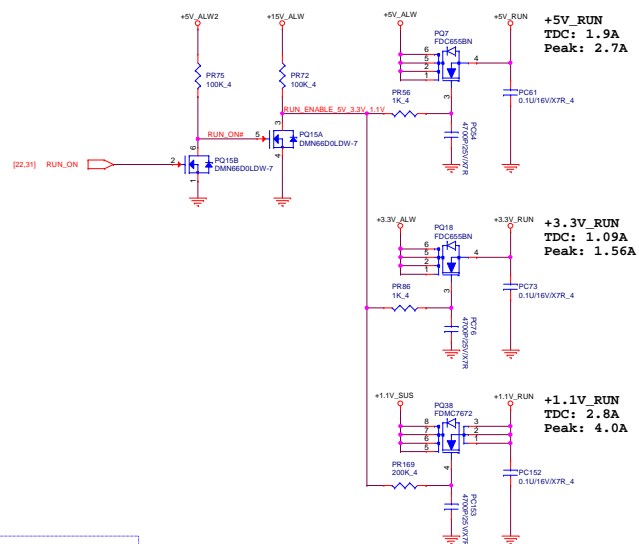
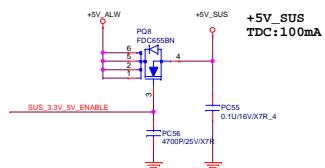
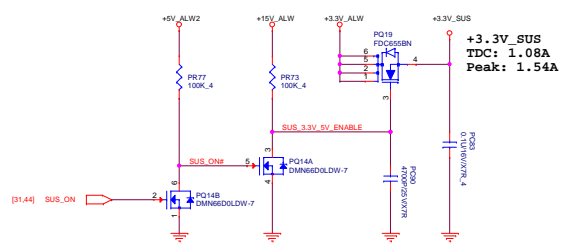
Size	Document Number	USB 3.0 Left	Rev B
Date:	Thursday, June 28, 2012	Sheet 38 of 55	

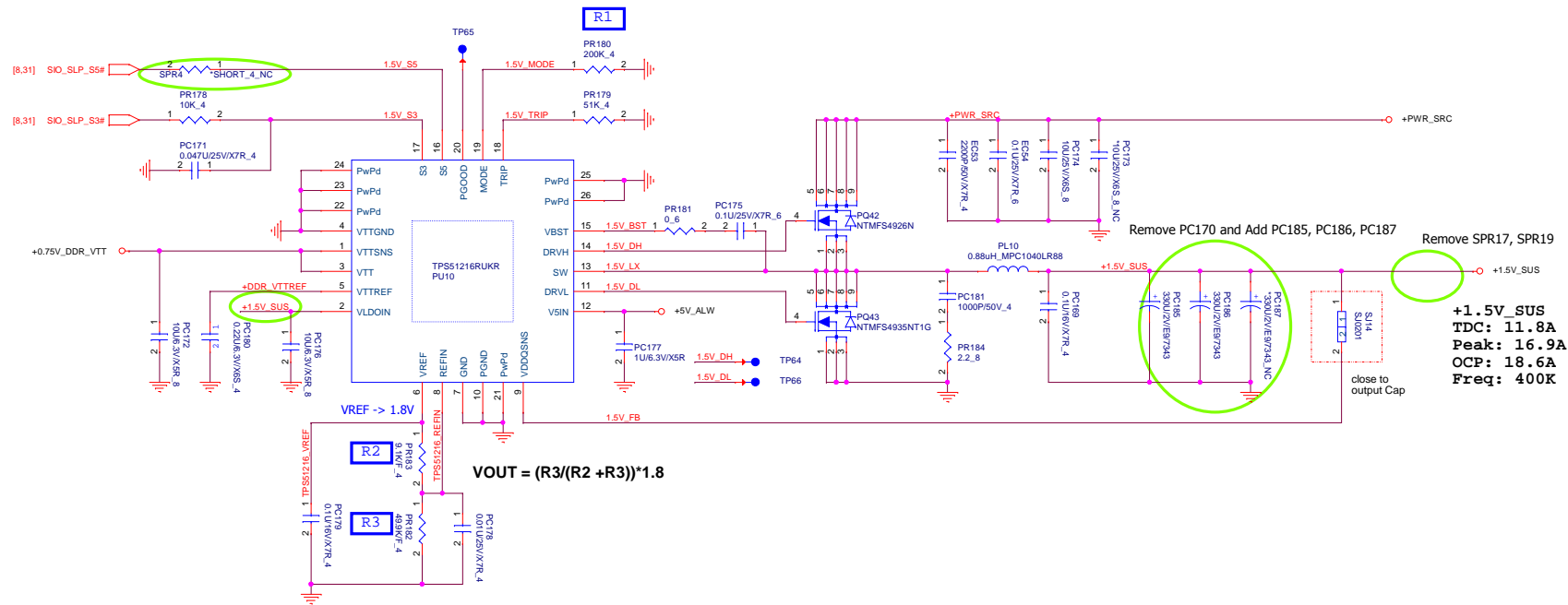
Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A



Register Address	Register Name
0x12H	ChargeOption()
0x14H	ChargeCurrent()
0x15H	ChargeVoltage()
0x3FH	InputCurrent()
0xFEH	ManufacturerID()
0xFFH	DeviceID()

<default>



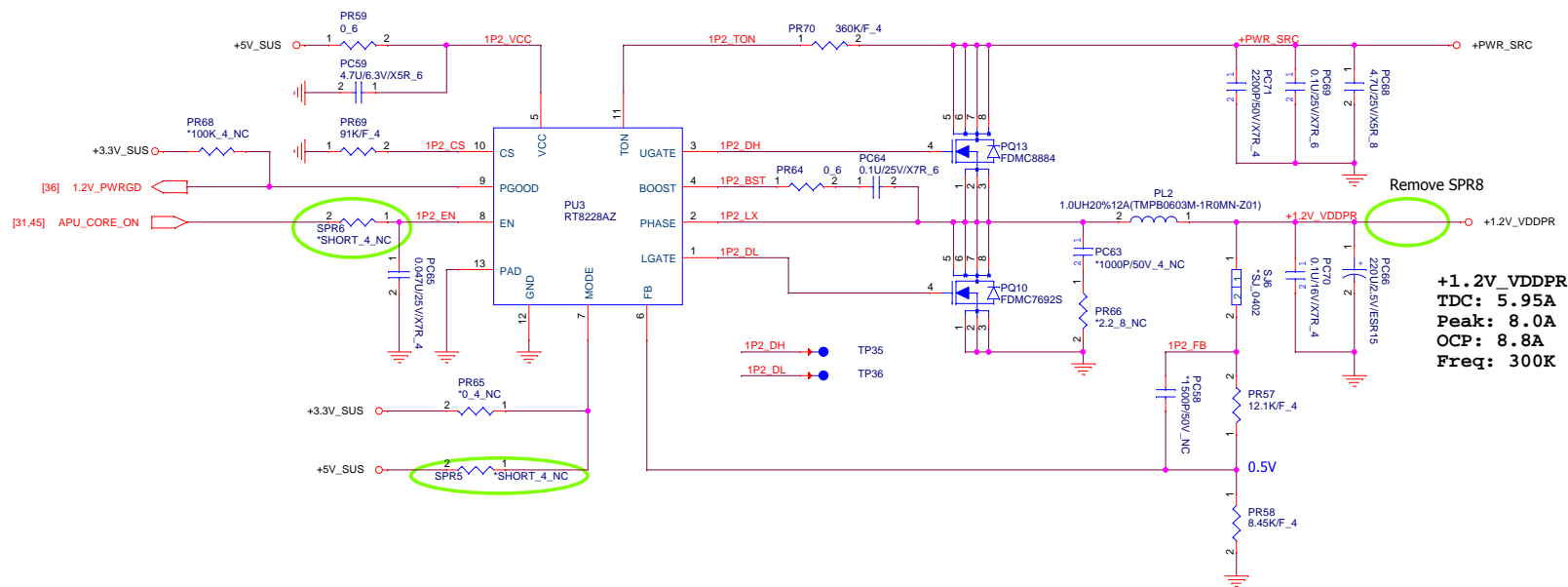


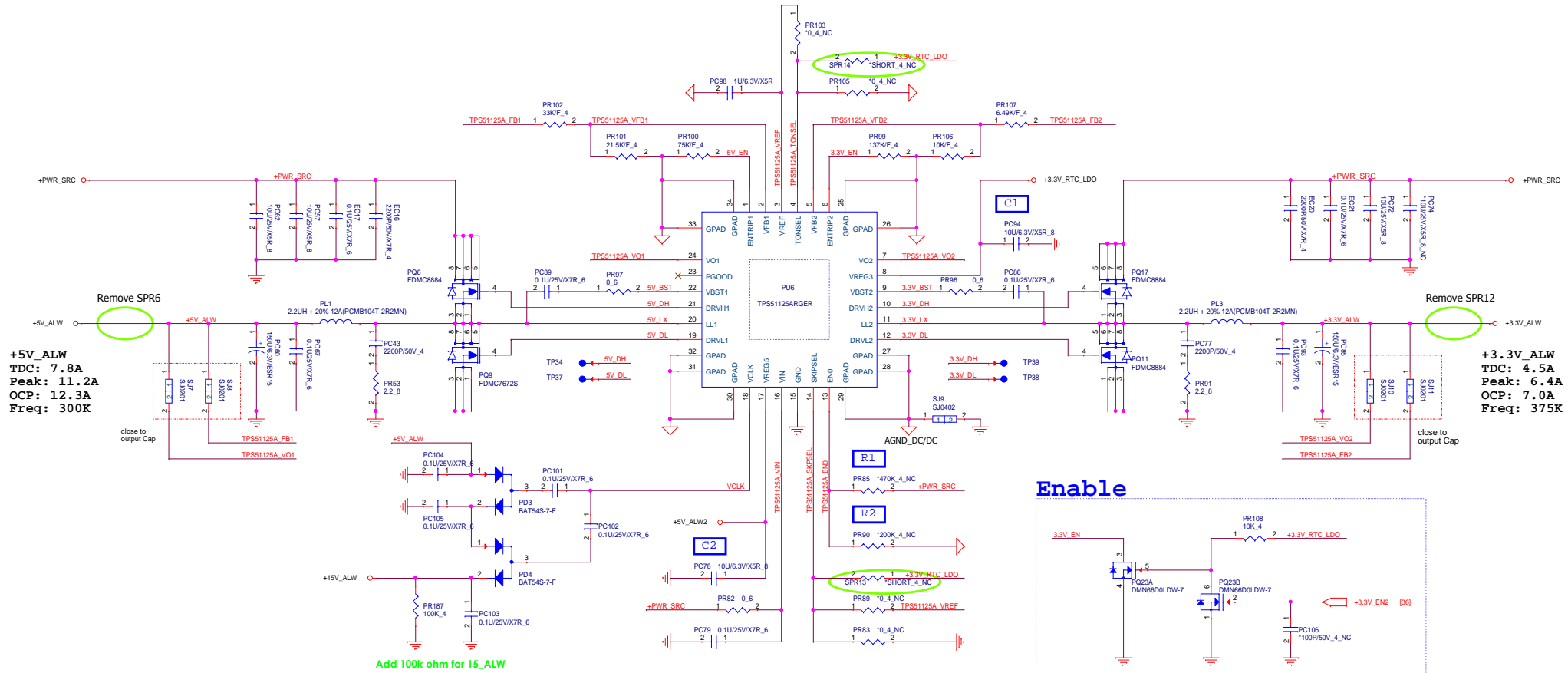
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection			
	Resistance between MODE and GND	Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz
R1	100K_4	CS41002JB20	300k Hz
R1	68K_4	CS36802JB12	300k Hz
R1	47K_4	CS34702JB21	400k Hz

		Quanta Computer Inc. PROJECT : R0AA	
		Document Number +1.5V_DDR0.75V(TPS51216)	Rev B



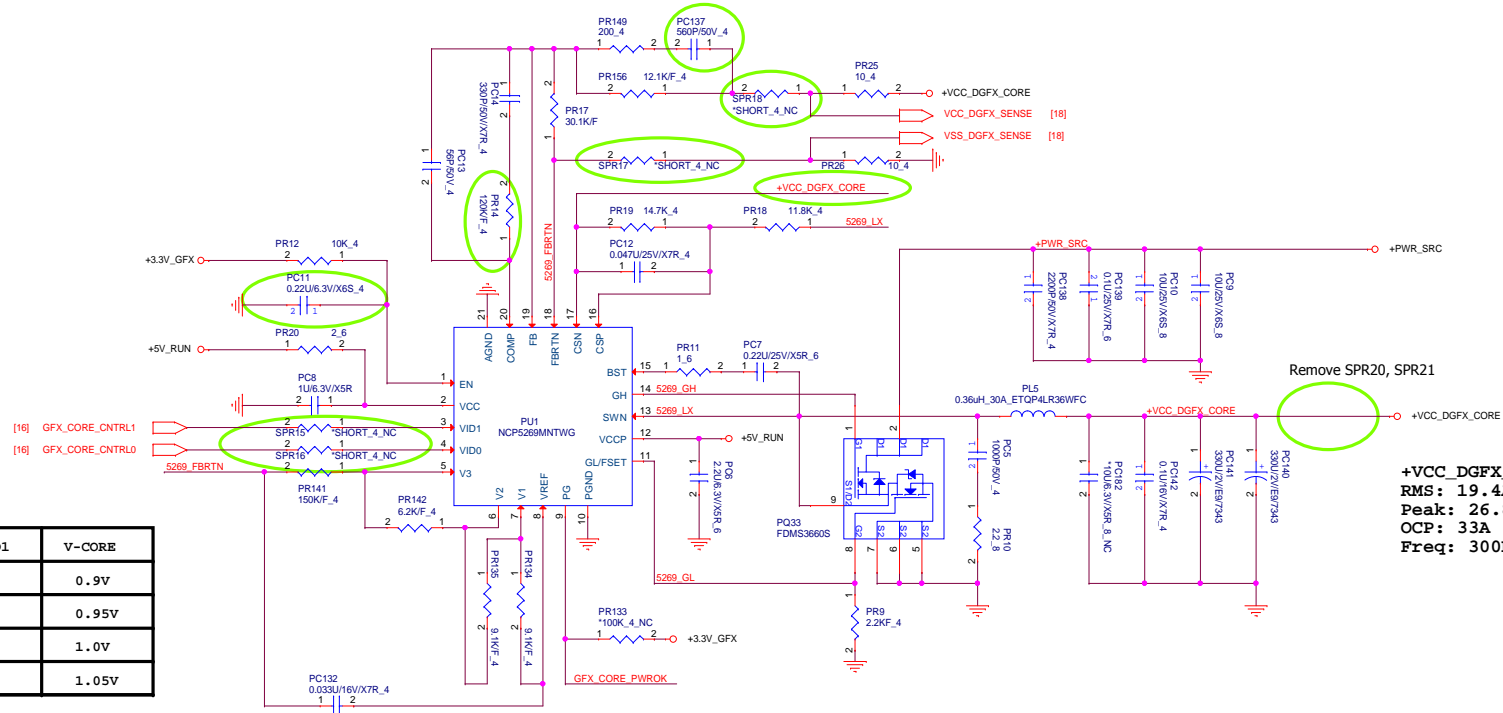


TPS51125A and RT8205N components differentia table

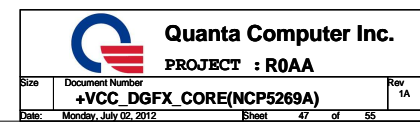
	TPS51125A	AL051125002		RT8205N	P/N not ready
R1	NC	N/A	R1	470K	CS44702JB15
R2	NC	N/A	R2	200K	CS42002JB14
R3	0_6	CS00003J951	R3	0_6	N/A
C1	10uF/6.3V_8	CH61001KA94	C1	4.7uF/6.3V_8	CH5471K1A00
C2	10uF/6.3V_8	CH61001KA94	C2	4.7uF/6.3V_8	CH5471K1A00
Q1	DDTA114YUA	N/A	Q1	DDTA114YUA	BA001140001
Q2	2N7002W-7-F	N/A	Q2	2N7002W-7-F	BAM70020040

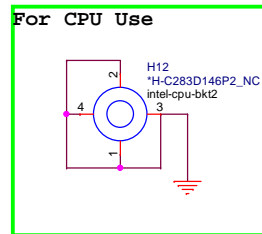
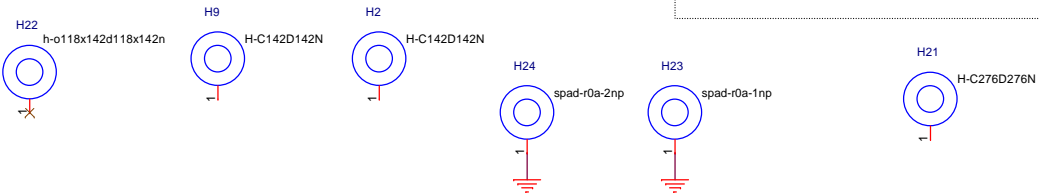
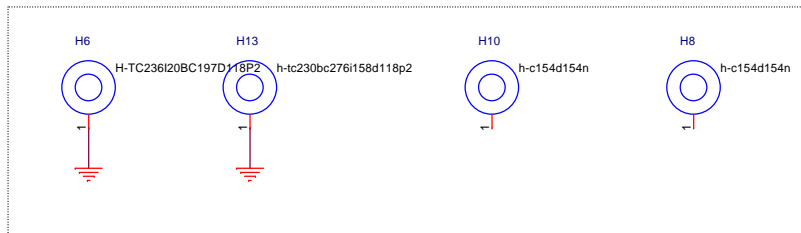
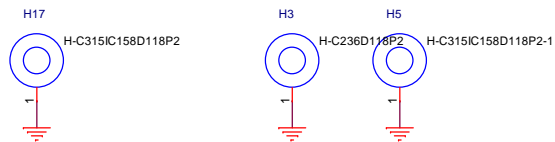
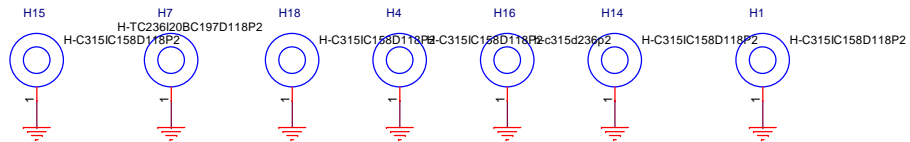
TPS51125A TONSEL Connection and Switching Frequency

	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz



+VCC_DGFX_CORE +/- 3%
RMS: 19.4A
Peak: 26.8A
OCP: 33A
Freq: 300K





Quanta Computer Inc.
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Size	Document Number	Rev B
SCREW PAD		
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